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SKA LFAA Subrack description document

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LIST OF ABBREVIATIONS

A..... Array Assembly phase n
AADC..... Aperture Array Design and construction Consortium
AAVS..... Aperture Array Verification System
AC..... Alternate Current
AD..... Analogue to Digital
ADC..... Analogue to Digital converter
AD-n ..... nth document in the list of Applicable Documents
ADD..... Architecture Design Document
ADU..... Analogue to Digital Unit
AIV..... Assembly Integration and Verification
API..... Application Programming Interface
APIU..... Antenna Power Interface Unit
ARM..... Advanced RISC Machine
ATE..... Automatic Test Equipment
AXI4..... Advanced eXtensible Interface 4
BOM..... Bill Of Material
C2C..... Chip to Chip
CBF..... Central Beamformer
CCB..... Configuration Control Board
CDR..... Critical Design Review
CI..... Configuration Item
CISPR..... Comité Internationale Speciale des Perturbations Radioelectriques
COTS..... Commercial Off the Shelf
CPF..... Central Processing Facility
CPLD..... Complex Programmable Logic Device
CM..... Configuration Manager
CMB..... Cabinet Management Board
CPU..... Central Processing Unit
CSP..... Central Signal Processor
DAQ..... Data Acquisition
dBm..... decibel to 1 mW power
dBFs ..... decibel to full scale
DC..... Direct Current
DDBH..... Digital Data Back Haul
DDD..... Detailed Design Document
DDR..... Double Data Rate (Memory)
DHCP..... Dynamic Host Configuration Protocol
DPLL..... Digital Phase Locked Loop
DRP..... Dynamic Reconfiguration Port
DSP..... Digital Signal Processing
DUT..... Device Under Test
DWDM..... Wavelength Multiplexing
ECP..... Engineering Change Proposal
EDA..... Engineering Data Archival (in TM)
EICD..... External Interface Control Document
EMC..... Electro Magnetic Compatibility
EMI..... Electro Magnetic Interference
ENOB..... Equivalent Number of Bits

ESD..... Electro-Static Discharge
F2F..... FPGA to FPGA
FAT..... Factory Acceptance Test
FE..... Front End
FFT..... Fast Fourier Transform
FN..... Front Node
FPGA..... Field Programmable Gate Array
FW..... Firmware
GbE..... Gigabit Ethernet
GTH..... Gigabit Transceiver?
GUI..... Graphic User Interface
HDL..... Hardware Description Language
HVAC..... High Voltage Alternate Current
HW..... Hardware
ICD..... Interface Control Document
IICD ..... Internal Interface Control Document
ILS ..... Integrated Logistic Support
INAF ..... Istituto Nazionale di Astrofisica
INAU ..... Infrastructure Australia
INFRA ..... Infrastructure
INFRAAUS ..... Infrastructure Australia
I/O..... Input/Output
IP..... Intellectual Property
IP..... Internet Protocol
IP2, IP3..... Intercept point to 2nd and 3rd harmonic
ISO..... International Organisation for Standardisation
IT..... Information technology
ITF..... Integration and Test Facility
LFAA..... Low Frequency Aperture Array
LFAA-DN..... Low Frequency Aperture Array – Data Network
LNA..... Low Noise Amplifier
LMC..... Local monitoring and Control
LRU..... Line Replaceable Unit
LCP..... Liquid Cold Plate
LVDS..... Low Voltage Differential Signal
M&C..... Monitor and Control
MAC..... Media Access Control
MCCS..... Monitor, Control and Calibration servers
MCU..... Micro Controller Unit
MTBF..... Mean Time Before Failure
MTTR..... Mean Time to Repair
MTU..... Maximum Transmission Unit
NTP..... Network Time Protocol
OA..... Operationally Capable
OHS..... Occupational Health and Safety
ORX..... Optical Receiver
OS..... Operating System
PBS..... Product Breakdown Structure
PCB..... Printed Circuit Board
PDR..... Preliminary Design Review
PCA..... Printed Circuit Assembly

PDS..... Power Distribution Subsystem
PFB..... Polyphase Filter Bank
PHY..... Physical (interface layer)
PLL..... Phase Locked Loop
PPE..... Personal Protective Equipment
PPS..... Peak per second
PRR..... Product Readiness Review
PSN..... Packet Sequence Number
PSS..... Pulsar Search
PST..... Pulsar Timing
PWM..... Pulse Width Modulation
QSFP..... Quad Small Form Pluggable
RAL..... Rutherford Appleton Laboratory
RAM..... Reliability Availability and Maintenance
RD-n ..... nth document in the list of Reference Documents
RF..... Radio Frequency
RFI..... Radio Frequency Interference
RFoF..... Radio Frequency signal over Fibre
RMON..... Remote Network Monitoring
RMS..... Root Mean Square
RoHS..... Restriction of Hazardous Substances
RPF..... Remote Processing Facility
SaDT..... Signal and Data Transport
SAFe..... Scaled Agile Framework
SDP..... Science Data Processing
SFDR..... Spurious Free Dynamic Range
SFP..... Small Form Pluggable
SKA..... Square Kilometre Array
SKA1..... Square Kilometre Array Phase 1
SKA1-Low..... SKA low frequency part of the full telescope
SKA1-Mid..... SKA low frequency part of the full telescope
SKAO..... SKA Office
SLD..... Single Line Diagram
SMB..... Subrack Management Board
S/N..... Signal to noise
SNR..... Signal to Noise Ratio
SOW..... Statement of Work
SPEAD..... Streaming Protocol for Exchanging Astronomical Data
SPI..... Serial … Interface
SPS..... Signal Processing Subsystem
SW..... Software
TCP-IP..... Transmission Control Protocol – Internet Protocol
TB..... Transient Buffer
TBC..... To Be Confirmed
TBD..... To Be Decided
TCP..... Transmission Control Protocol
TM..... Telescope Management
TPM..... Tile Processor Module
UCP..... Uniboard Control Protocol
UDP..... User Datagram Protocol
UTC..... Universal Time Coordinated

VGA..... Variable Gain Attenuator
VHDL..... VLSI Hardware Description Language
WBS..... Work Breakdown Structure
WDM..... Wavelength Division Multiplexing
WEEE..... Waste Electric and Electronic Equipment
XML..... Extensible Markup Language



1 Purpose of the document

The purpose of this document is to describe at a high level of details the Subrack structure of LFAA Signal Processing System (SPS) cabinets and the rationales for its development.

In brief, it is an integrated system that matches LFAA standards, features limited cabling and fits in a standard 6U, 19” chassis.

It can be tested on a bench, and once integrated and tested it can be simply packed and shipped.

2 Reference documents

2.1 Project documentation

[PD1] LFAA Signal Processing System Detailed Design Document, SKA-TEL-LFAA-0500035, Issue 1
[PD2] LFAA Signal Processing System Prototype Test Report, SKA-TEL-LFAA-0500047, Rev. 01
[PD3] SKA LFAA SPS Cabinet Specification Document, Issue, 1 04/04/2018, Sanitas EG
[PD4] SKA LFAA conceptual sub-rack design, Issue 1.2, 14/02/2018, Sanitas EG
[PD5] SKA Management Board Description, Issue 1.1, 24/20/2019, Sanitas EG
[PD6] Cabinet Monitor and Control Points, Issue 1, 15/11/2018, Sanitas EG
[PD7] Design of performance improvements and industrial process of SKA-LFAA receiver , LEONARDO
[PD8] SKA iTPM-ADU V1.6 Board User Manual, Issue 1.1, 20/02/2020, Sanitas EG
[PD9] SKA System Budget-Low System Timing Budget_u1, SKA-TEL-SKO-0000637-03
[PD10] Clock Distribution Analysis, Issue 1, 15/11/2018, Sanitas EG
[PD11] Detailed Thermal Study Cooling Solution for SKA, Rev. 12, AAVID Themalloy
[PD12] SKA Backplane Board, Issue 1.1, 23/09/2019, Sanitas EG
[PD13] R. Chiello, iTPM Firmware Architecture, Issue 2.2, 18/05/2020, University of Oxford
[PD14] G. Comoretto, C. Belli: LFAA Tile Beamformer Signal processing, INAF
[PD15] G. Comoretto, LFAA SPS Network, Rev 2.2, 30/01/2020, INAF

2.2 Public regulations, standards and data sheet

[PS1] PET1300-12-054xA AC-DC Front-End Power Supply, Bel Power Solution and Protection, datasheet, available at https://www.belfuse.com/resources/datasheets/powersolutions/ds-bps-pet1300-series.pdf

3 Overview of SPS Subrack/Cabinet

This section describes the structure of LFAA SPS Subracks. Constituents are detailed in the following sections.

The context in which the SPS Cabinets and Subrack are installed is shown in Figure 1. It represents the Product Breakdown Structure (PBS) for the Low Frequency Aperture Array, highlighting all its components up to level 4.

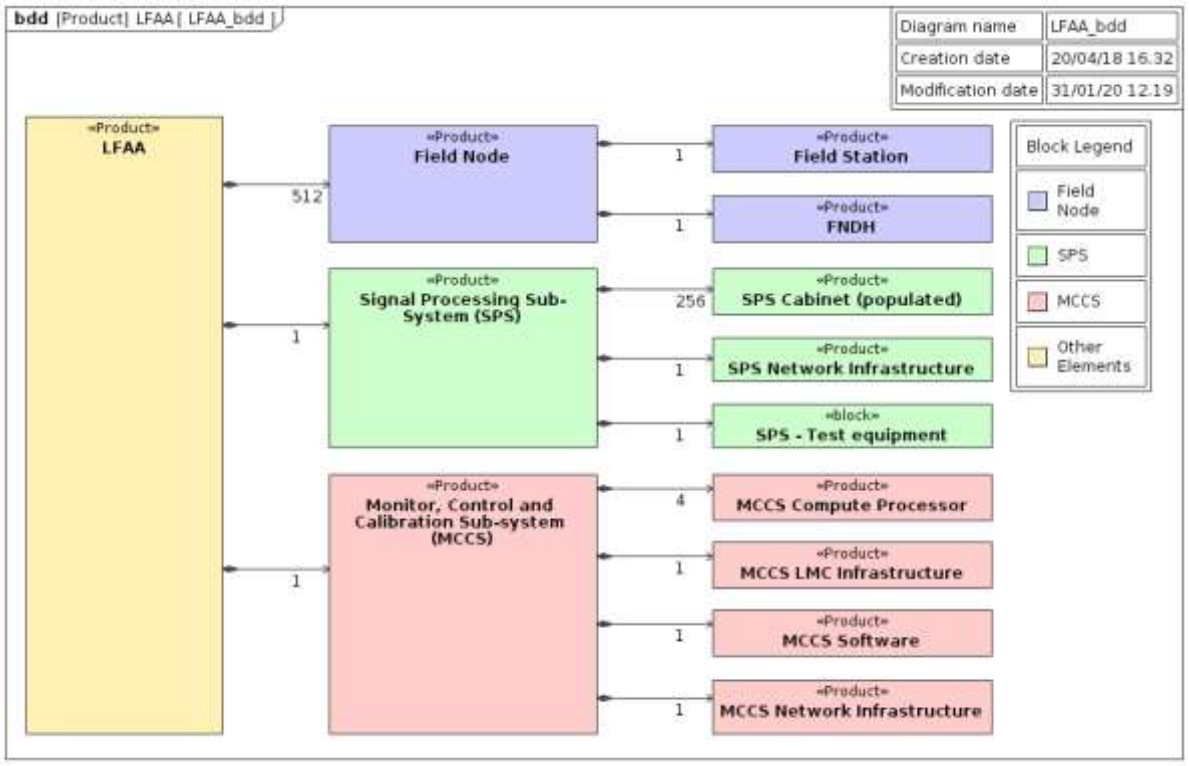


Figure 1 LFAA - Product Breakdown Structure.

The SKA LFAA analogue chains deliver several thousands of optical fibres, each carrying two analogue optical signals coming from the antennas installed in the desert area to a central processing facility and to the remote stations.

A special infrastructure is provided for the central processing facility and remote stations for the acquisition and processing of the signals. A common cabinet system has been designed for both locations that contains the required acquisition electronics and related functions.

Summarizing the main requirements needed for these infrastructures are:

- Tile Processing Module (TPM) boards are the basic element, receiving 32 signals each with 16 WDM receivers, standard 6U rack mount size
- 256 single side cabinets containing 32 TPMs each (8200 TPM total)
- Clock distribution network from a single source to each cabinet with a 10 MHz and 1 PPS signals
- Control/data network based on 40G and 10G optical/copper (QSFP+) cabinet level links

- Three-phase 360V AC power supply
- Cooling system.

The TPM is the main sub-system of the LFAA signal processing system. This is a rack-mounted unit that processes the signals from 16-antennas (32-signal chains). The TPM receives the analogue signals from the RF antenna amplifiers, as analogue RF over Fibre optical signals, amplify and filter them (RF conditioning), convert them in digital form and digitally process them to form station beams. 16 Tile Processing Modules related to one station are connected using a high-speed data switch. Partial beams are sent along a chain of 16 TPMs, with each TPM combining the internally generated partial beam with the travelling one. The final station beam is then sent to the central processing facility.

The data switches are used also to interface the TPM to the monitor, control and calibration servers, both for local monitor and control functionalities and for sending to these server calibration samples to be stored in the transient buffer. A block description of the TPM is shown in Figure 2.

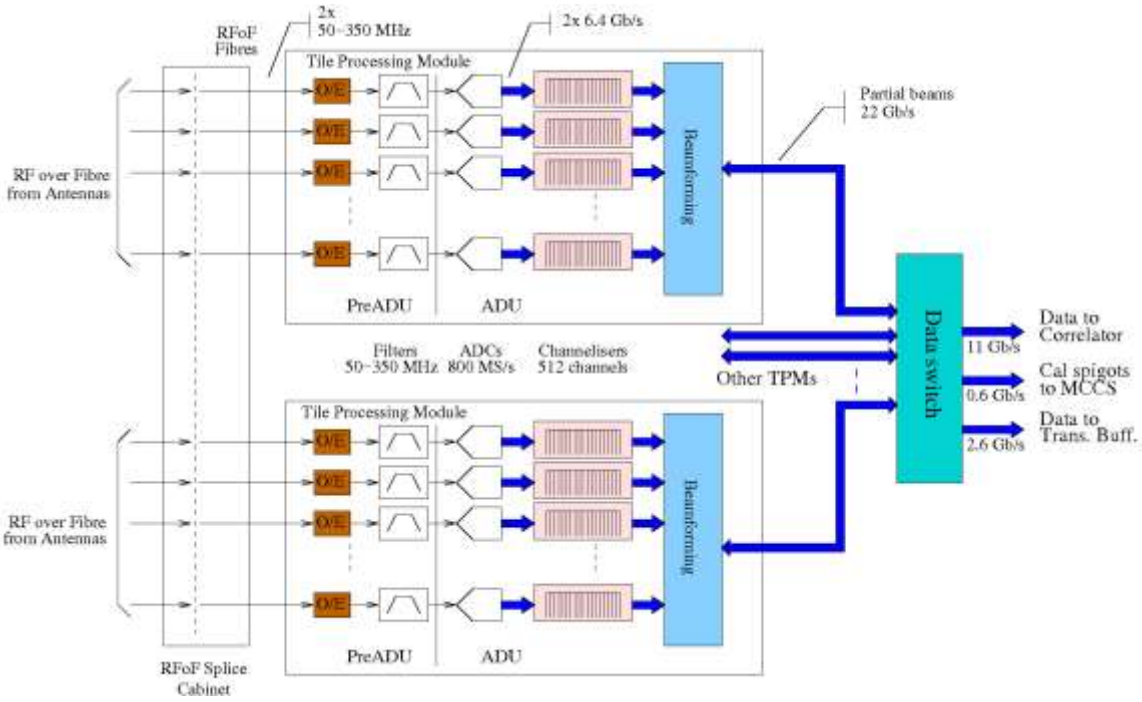


Figure 2 Block description of the TPM.

SPS is physically implemented in 256 cabinets. Each cabinet hosts 32 TPMs and 2 data switches, for two stations, plus the necessary power, cooling, clock distribution and management hardware.

The cabinet design takes into account several design criteria, both typical of a large installation and specific, in consideration of the target location, which is the middle of the Australian desert, in particular energy efficiency, cost, reliability and maintenance.

An integrated and rather compact subrack based solution has been conceived for LFAA cabinets in order to meet the stated requirements. The following elements are present:

- Cooling system
- Cabinet management board unit

- Four subracks containing 8 TPMs each
- 40G Ethernet switch
- AC Power distributor.

Figure 3 shows the product breakdown structure of the SPS Cabinet. The diagram goes up to level 7 showing also the components of the TPM Subrack and the main elements composing the TPM.

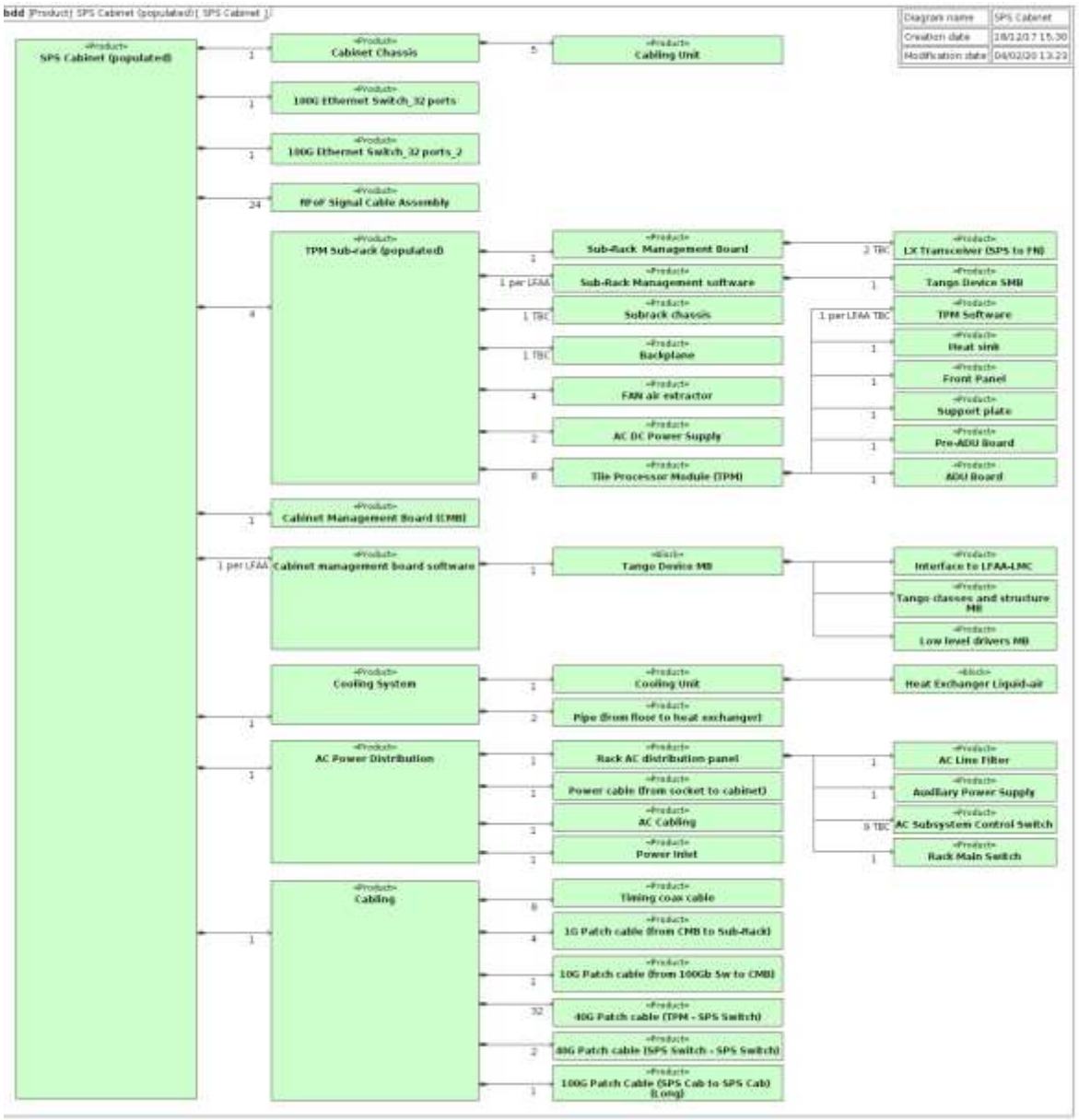


Figure 3 SPS Cabinet - Product Breakdown Structure.

The proposed cabinet uses standard cabling and mechanical interface to achieve a robust design and testability, which means each cabinet module can be fully tested as stand-alone element. Standard cabined solutions, such as VARISTAR or RITTAL, with air cooling system provides the needed characteristics at reduced costs [PD3].



A subrack integrates 8 TPM boards each with local management functions, namely power supply, clocks and Ethernet [PD4].

A Subrack Management Board (SMB) has been realized for this purpose. The SMB provides a backplane for connecting and managing multiple TPMs with a sub-rack. It acts as a distribution board for power, network and other signals such as clock and PPS [PD5].

Since it distributes power, it allows for control of power output to the TPMs and exposes the functionality to remotely switch on and off TPMs, as well as provide measured power consumption. Apart from TPM-related functionality, the board itself needs to be monitored and controlled, such that temperature as well as voltage and current use of the board are exposed. The SMB provides however some safety related functionalities, switching off any component in the subrack which exceeds predefined safety margins (overcurrent, overvoltage, temperature). Monitor and management resources available in the SMB are described in [PD6].

Thanks to the functions and connections allocated to subracks, the resulting cabinet level connections and cabling are simplified. Furthermore, this architecture simplifies the heat dissipation, and installation/maintenance.

The proposed subrack design satisfies the following general specifications:

- Standard 19” format, 6RU vertical spacing and 541mm horizontal depth
- AC supply input with at least 1.2KW (220V or 360V)
- One reference and PPS clocks
- One copper gigabit Ethernet for management interface
- 16x8 RFoF (RF over Fibre) for TPMs analogue inputs
- 8 40G Ethernet interfaces for the TPM data.

Figure 4 shows the flow of information and physical quantities (heat, power) among the elements composing the Cabinet. Different colours have been used to distinguish between the nature of the interface (mechanical, thermal, power, signal).

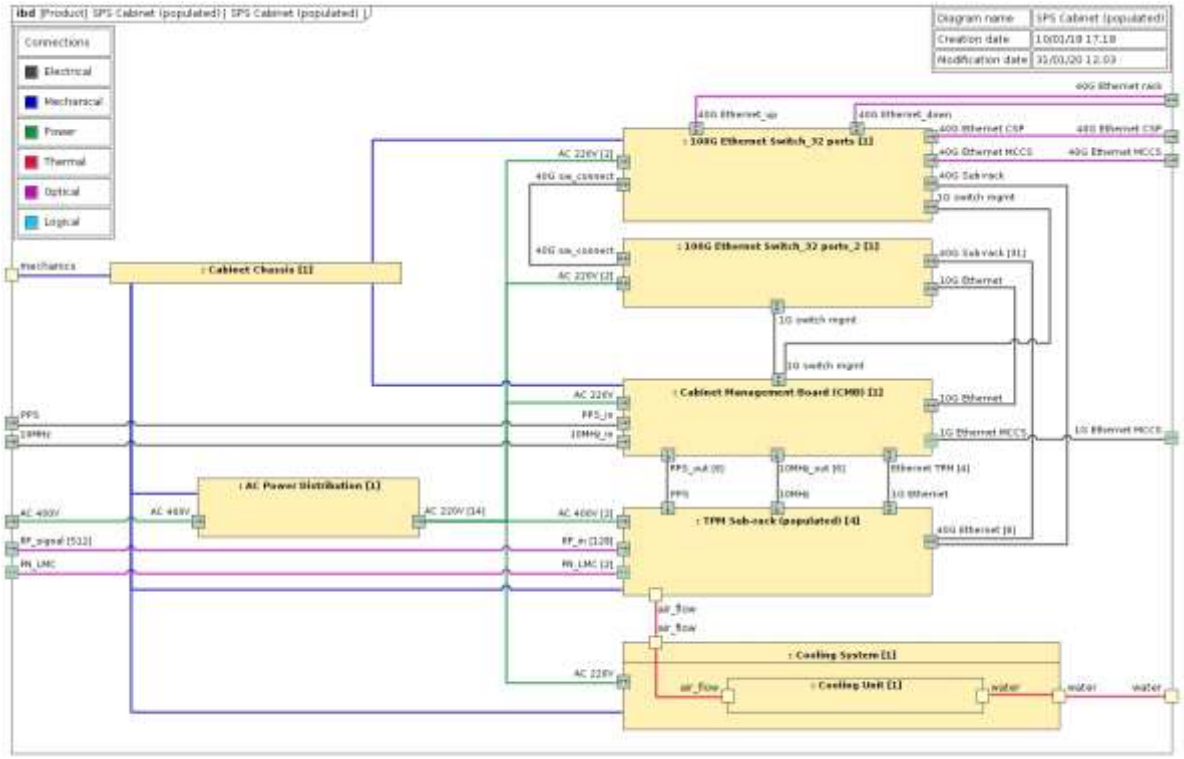


Figure 4 Internal interconnections - SPS Cabinet.

4 Research institutes and industries involved

Bologna Institute of Radioastronomy, Catania Astrophysical Observatory, Arcetri Astrophysical Observatory, Milan Space Astrophysics and Cosmic Physics Institute, Leonardo Finmeccanica, Sanitas EG and AAVID Thermalloy.

5 Subrack Mechanics

The main structure of the Subrack is a standard 6U, 19” chassis “europacPRO” from Schroff (Figure 5).

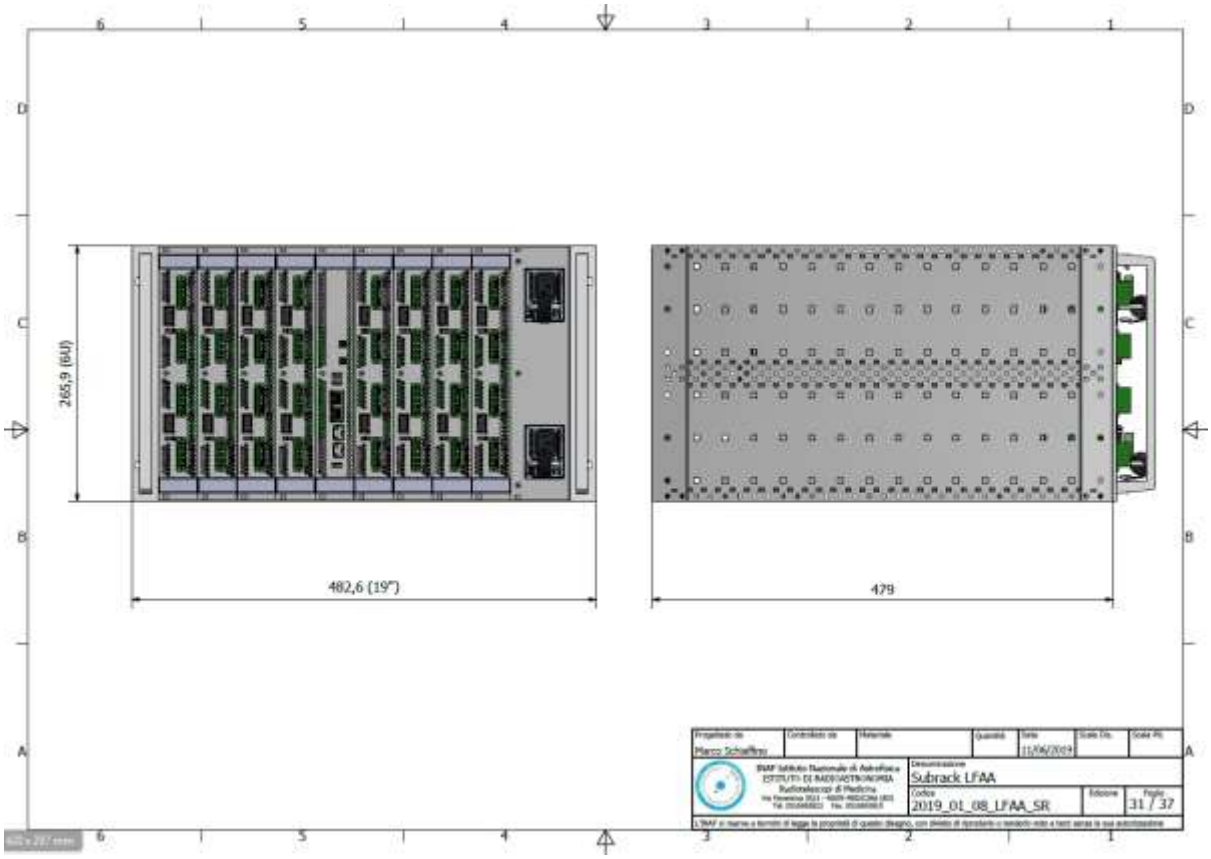


Figure 5 External dimensions of the Subrack.

Standards and certification of the europacPRO Subracks are:

- Internal and external dimensions in accordance with:
  - IEC 60297-3-101 / IEEE 1101.1
  - IEC 60297-3-102 / IEEE 1101.10/11
  - IEC 60297-3-103
- Type of protection IP20 in accordance with IEC 60529
- EMC testing in accordance with VG 95373 part 15
- Shock and vibration test report:
  - Railway standards BN411002; BN411003, NFF 61005, NFF60002
  - IEC 61587-1, EN 50155

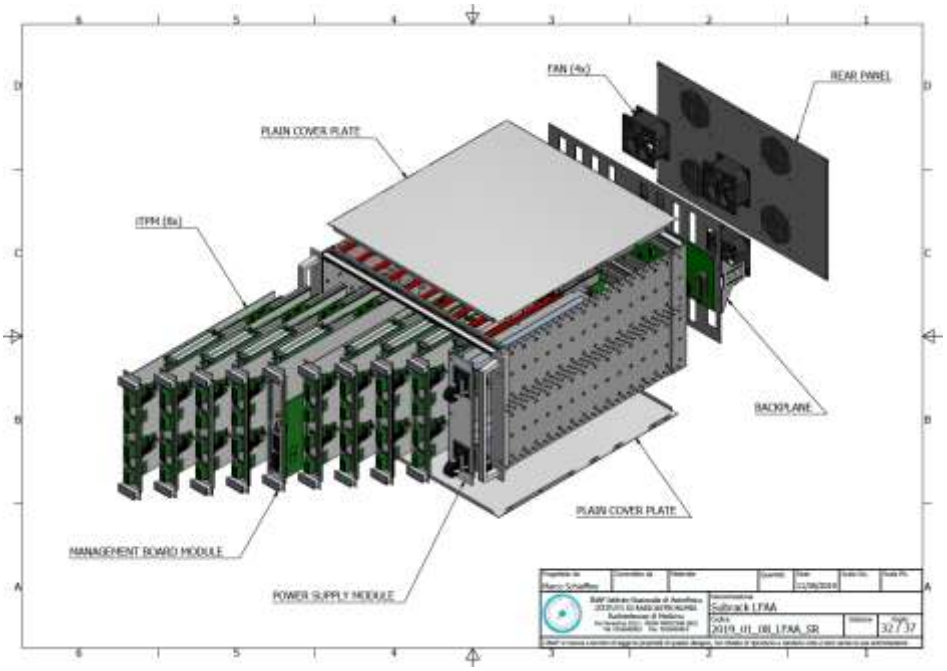


Figure 6 Detailed view of the Subrack.

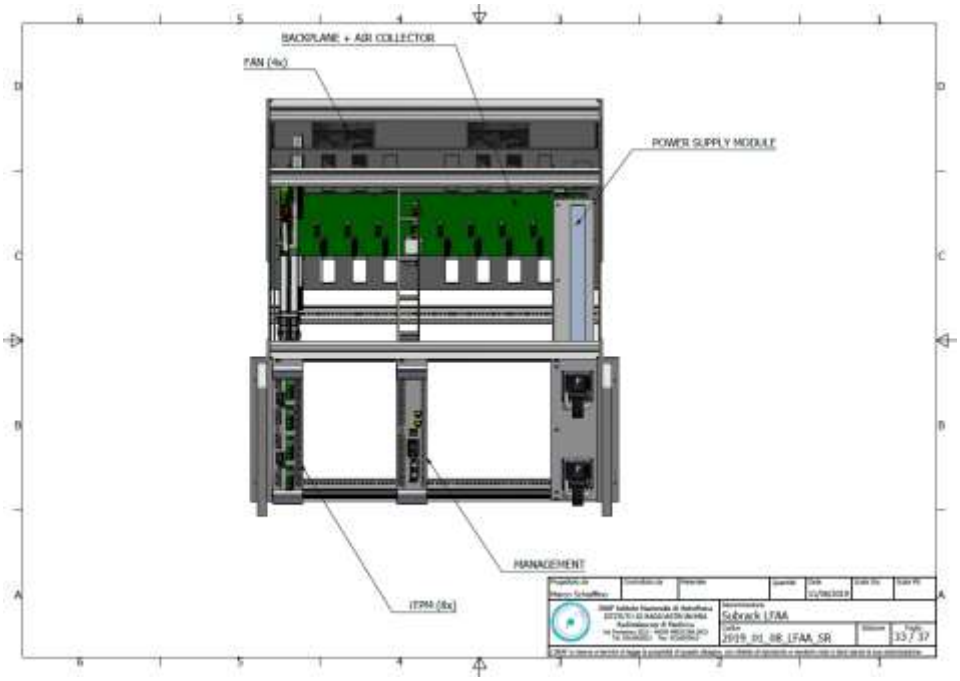


Figure 7 Back view of the Subrack.

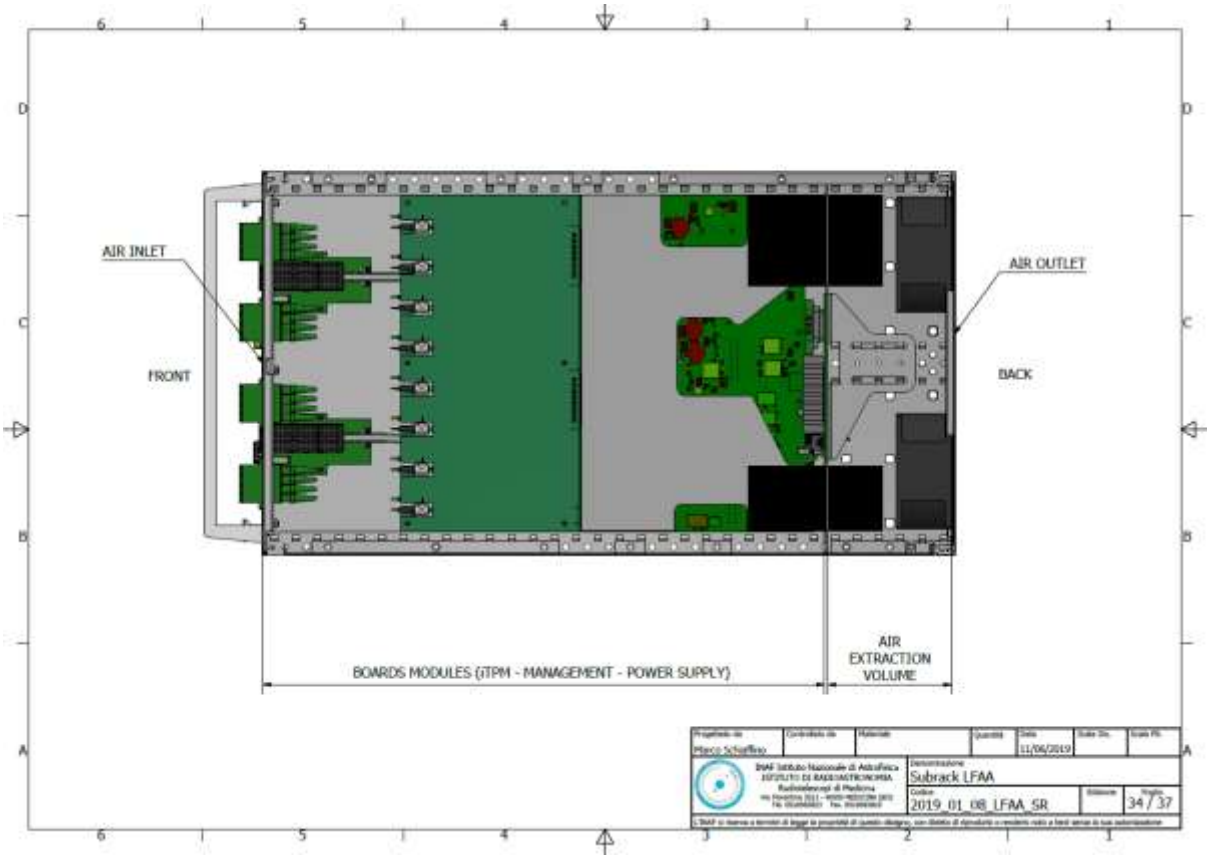


Figure 8 View from the above of TPM 1.5 with mounted heatpipe on the right.



6 Cooling System

The cooling solution designed for the SPS equipment is a heatpipe system, a phase change structure directly attached on each board. This configuration eliminates any mechanical contact between the cooling system and the internal structure of the subrack once the board are inserted, avoiding additional interface connections that might slow down the heat transfer and consequently the efficiency of the cooling solution.

This new solution is described in the following sections.

6.1 Design

The subrack unit include 8 TPM boards, 1 power supply unit and 1 subrack management board, with a power of 800 W equally distributed on each board:

- PTPM ≈ 100 W for each board
- PSUB-RACK ≈ 800 W for each subrack[1].

Subrack will be cooled with an air solution.

Each heapipe system includes:

- 1 Aluminium base obtained by CNC machining
- 4 Flattened heatpipes inserted into the machined grooves of the aluminium base
- 2 Fin Packs.

The entire cooling solution is assembled together through soldering, a welding process obtained in the oven at 200°C that creates a metal junction in between the components to ensure the heat transfer.

This solution was designed by AAVID Thermalloy [PD11]. The same company proposed the solution in the cabinet preliminary design based on liquid cooling.

Thermal grease or a soft silicon material is recommended in between the electrical components and the aluminium base in order to avoid any air gap and ensure a proper heat transfer.

[1] This value does not account for pre-ADUs (≈16 power budget), as they are not involved in heatpipe consumption.

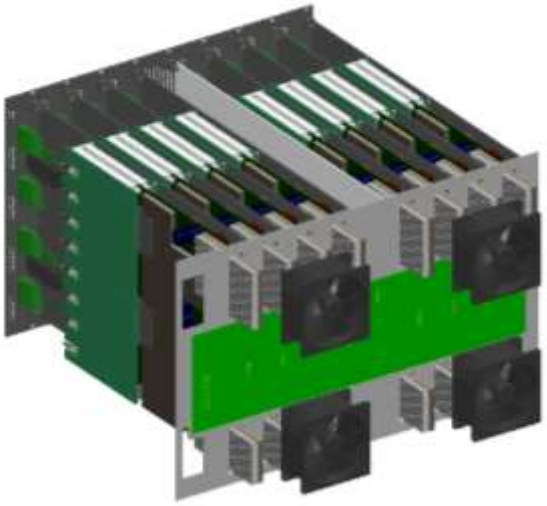


Figure 9 Extractable heatpipe pipe system.

The heatpipe system is mounted on the board and conveys the heat towards a fin pack, which is included in the system. A part of the fin pack protrudes from the board and directly receives the airflow from an air collector being channelized in between the fins.

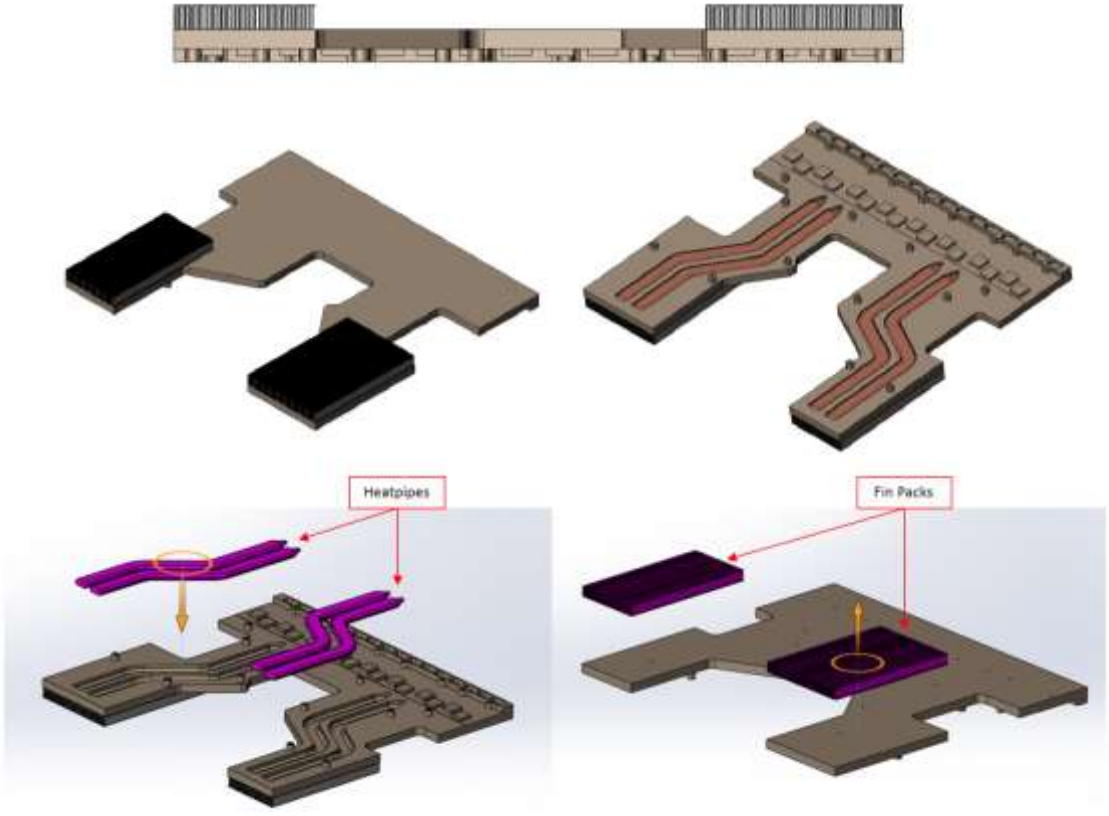


Figure 10 Picture of the heat pipe mounted on the board; vertical section (uppermost) and top site (lowermost).

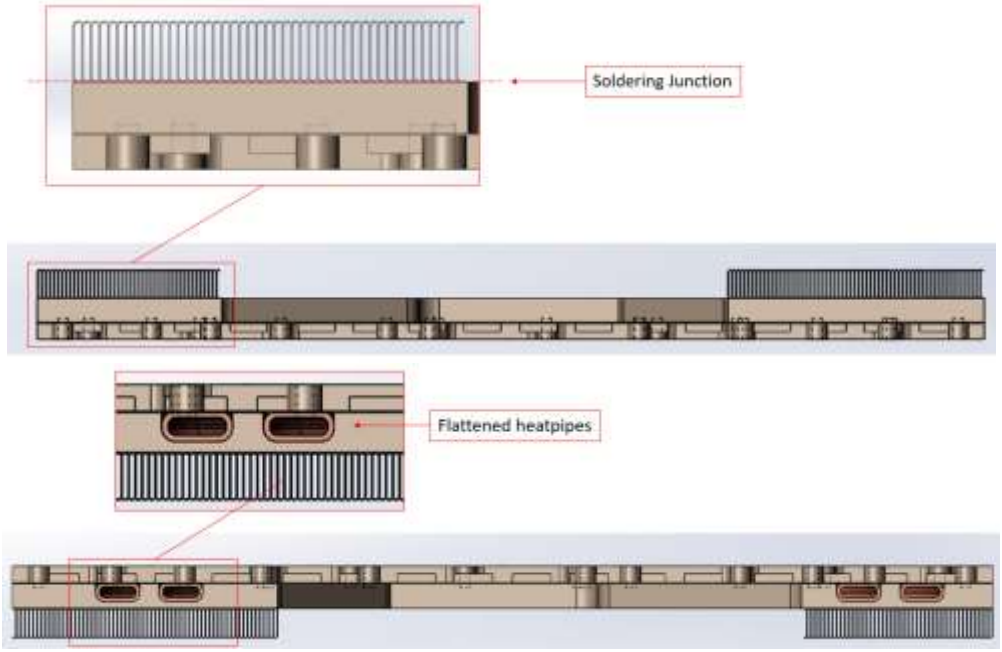


Figure 11 Picture of the heat pipe mounted on the board; bottom site.

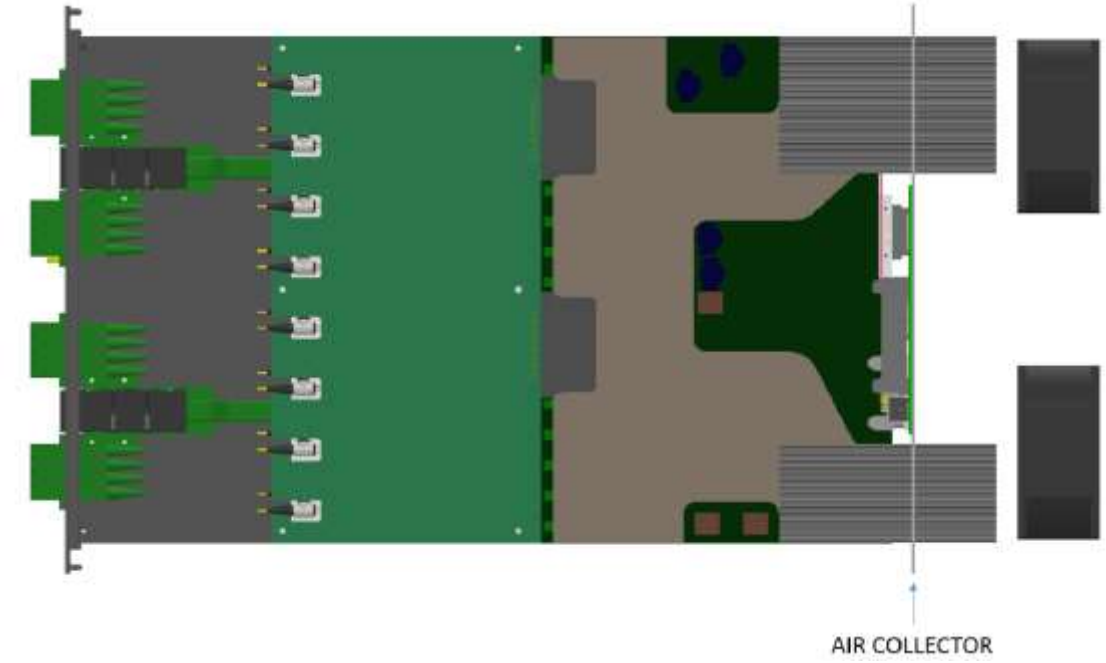


Figure 12 View from the above of the heatpipe mounted on the TPM; the ADU board can be recognized on the right, while the pre-ADU board is on the left.

The heat dissipation process is indicated below: transfer process is

1. Heat coming from the electrical components flows through the aluminium plate and overheats the closer extremity of the heatpipes
2. Once warmed up, water inside the heatpipe evaporates creating an evaporation area

3. The vapour consequently flows by gas diffusion to the other extremity where the fin packs are located
4. The vapour condensates due to the reduced temperature in the area, releasing the heat to the fins. Liquid water flows back by capillarity to the evaporation area
5. Heat transmitted to the fins is released into the air blown by the fans, cooling down the fins
6. Heated air flows into the radiator of the chiller to be cooled down

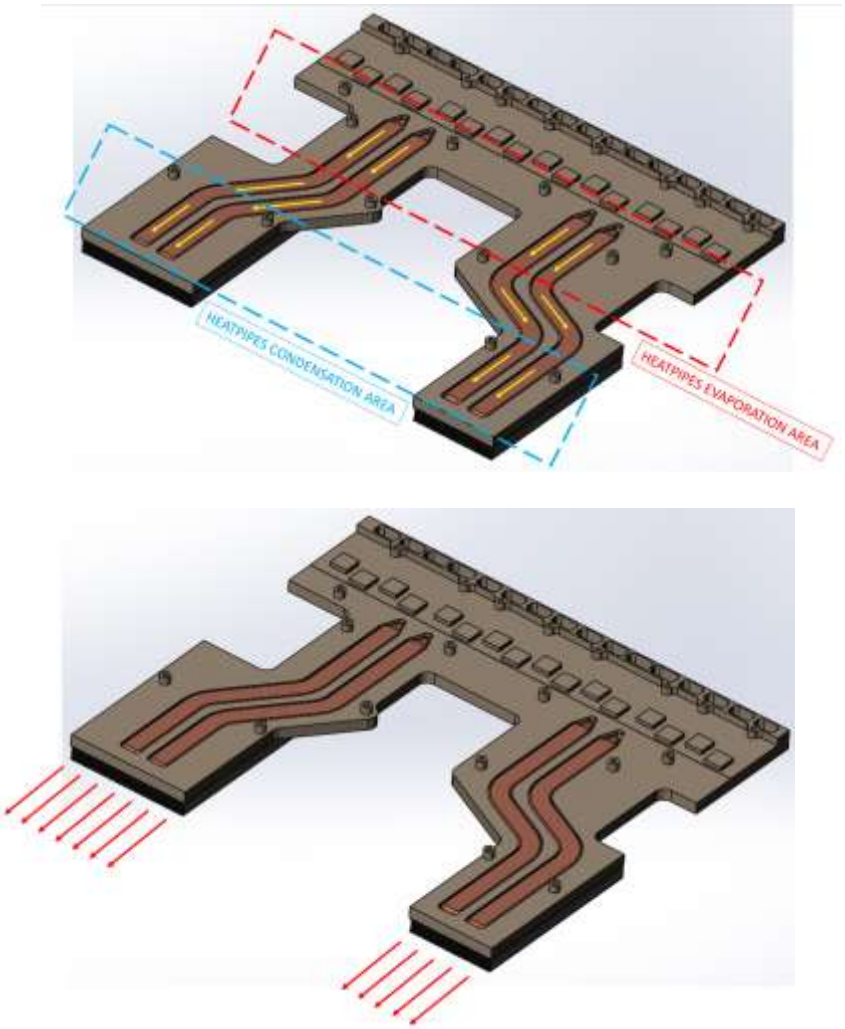


Figure 13 Heat dissipation process in the heatpipe.

6.2 Simulation results

The ambient temperature considered for the cooling system is 40 °C. Detailed simulation results, given in Figure 14 and Figure 15, show that the maximum temperature on the heatpipe system under the components is 61.8 °C [PD11].

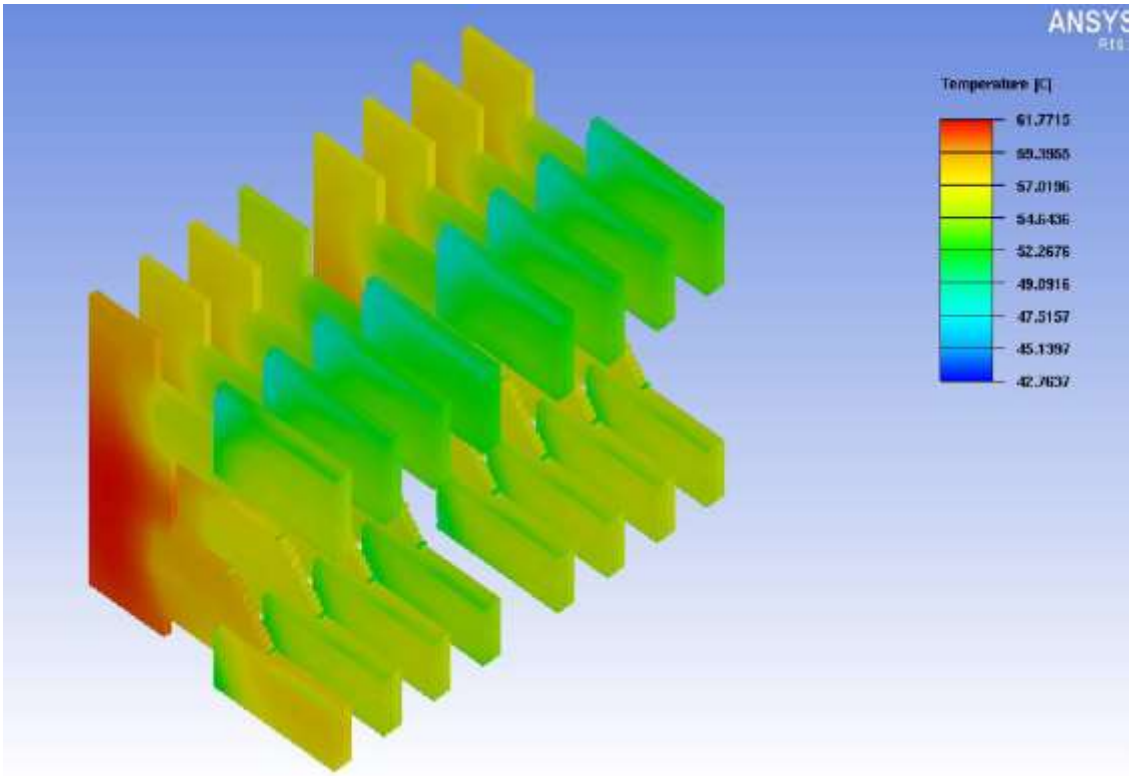


Figure 14 TPM Subrack thermal performance, front view.

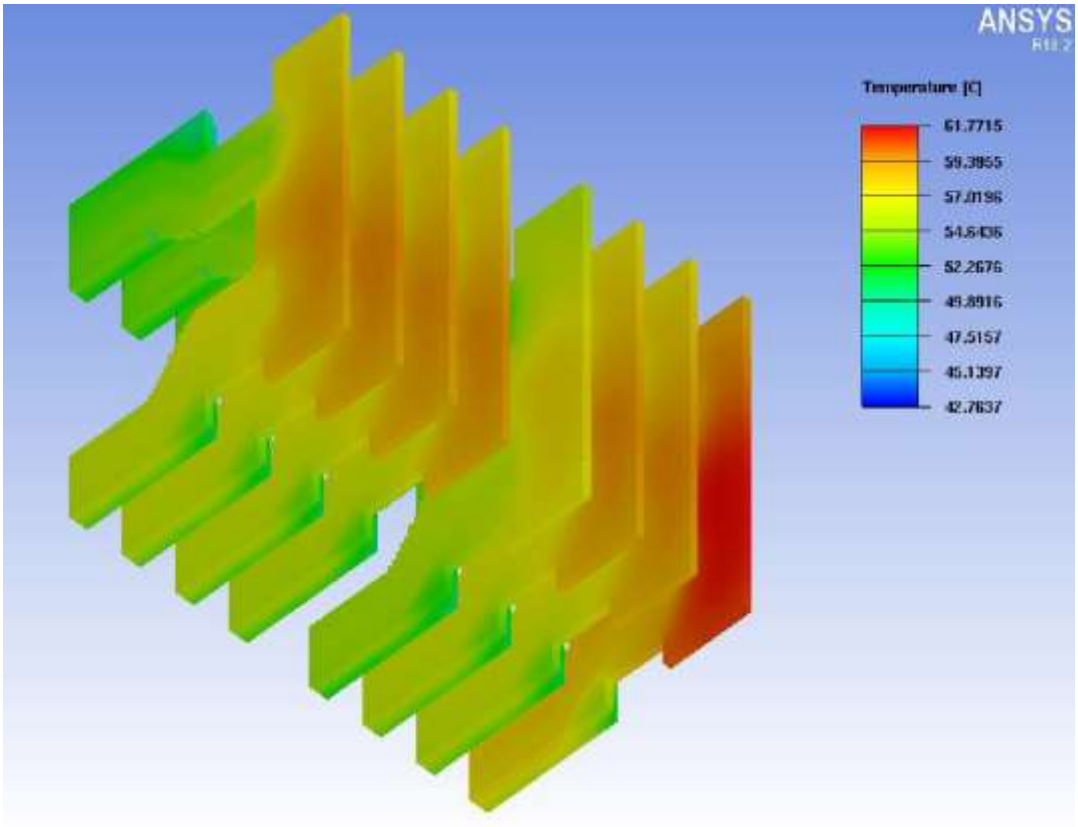


Figure 15 TPM Subrack thermal performance, back view.

Table I Extractable heatpipe system performance.

SOLUTION	T_{AMB} [°C]	T_{MAX} [°C]
Extractable Heatpipe System	40	61.8

Due to the typical precision of a simulation, an error of 5-10 % should be considered. It is strongly recommended to validate thermal calculation by testing prototype.



7 Subrack Interfaces

Subrack Interfaces are grouped on the front side with pluggable standard connectors and are all removable in the normal operation without halting the system.

The power interfaces are on the right side with two standard 220V ATX power interface. The two power supplies can work in parallel with shared load or stand alone as single power unit. Standard power modules can be replaced with compatible and verified ones.

The management interfaces are in the subrack middle area connected with the management board. They include: synchronizations, 2x RJ45 10/100/1000 Ethernet, 2x SFP gigabit Ethernet fibre interface, 3x4 status and user led.

The TPM interfaces are, for each TPM: 16 optical LF fibre connectors and 2 QSFP connectors for 40G Ethernet or 4x10G Ethernet, 2x4 TPM status LEDs.

Characteristics are summarized in Table II.

Table II Subrack Interfaces.

Description	Direction	Numbe	Type	Connector
Power Input	IN	2	AC 220V, 16A, 50/60 Hz	ATX power cord
Synchronization, 10 MHz Reference Clock	IN	1	Signal 50 ohm, 8-12 dBm (*1)	SMA
Synchronization, PPS	IN	1	Signal 50 ohm, CMOS 3,3V	SMA
Analogue signal from antennas RFoF	IN		Optical RFoF	LC
Acquisition Data	IN/OUT	2	4x10Gb or 40Gb Ethernet (*2)	QSFP
Control link	IN/OUT	2	10/100/1000 Gigabit Ethernet	RJ45

*1 The 10 MHz reference signal shall respect TBD noise spectra specification to guarantee the TPM acquisition performances

*2 Ethernet Link Type is related to the application firmware loaded on the TPM FPGAs

For interfaces among constituents, that is Subrack Management Board, Cabinet Management Board, TPM, Backplane and supply unit, please refer to [PD3]-[PD5], [PD8] and [PD12]

Figure 14 analyses the physical interconnection among elements composing the Subrack, showing with different colours the various types of interfaces.

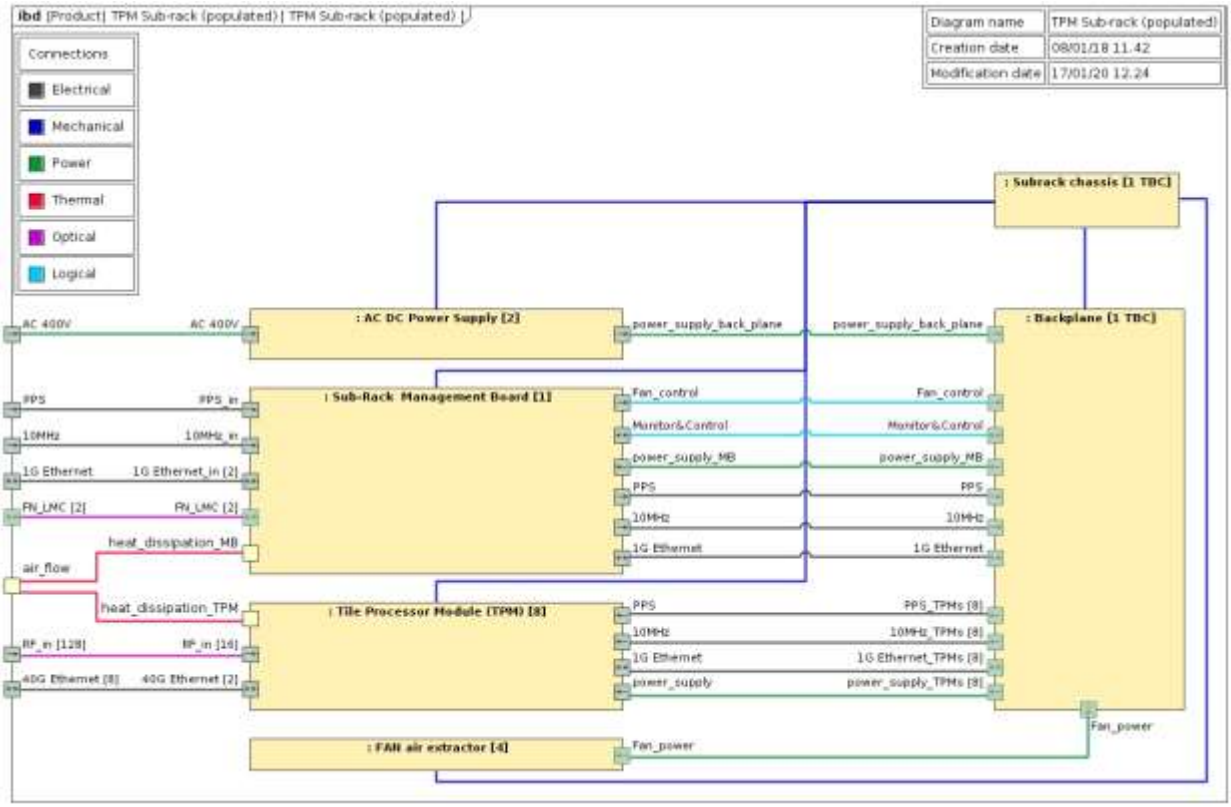


Figure 16 Internal interconnection - TPM Subrack.

Subrack status LEDs are organized as follow to facilitate user maintenance:

- 4 Subrack general status LEDs, 2 RED and 2 GREEN to show Power presence, system running and global operativity (e.g. PLL Lock status)
- 8 Subrack TPM LED, BICOLOR, to specify TPM power ON and TPM operative status.

TPM Status LEDs are associated to each 40G QSFP Connector, single colour, are user programmable to indicate general board status, 40 G link status, TBC.

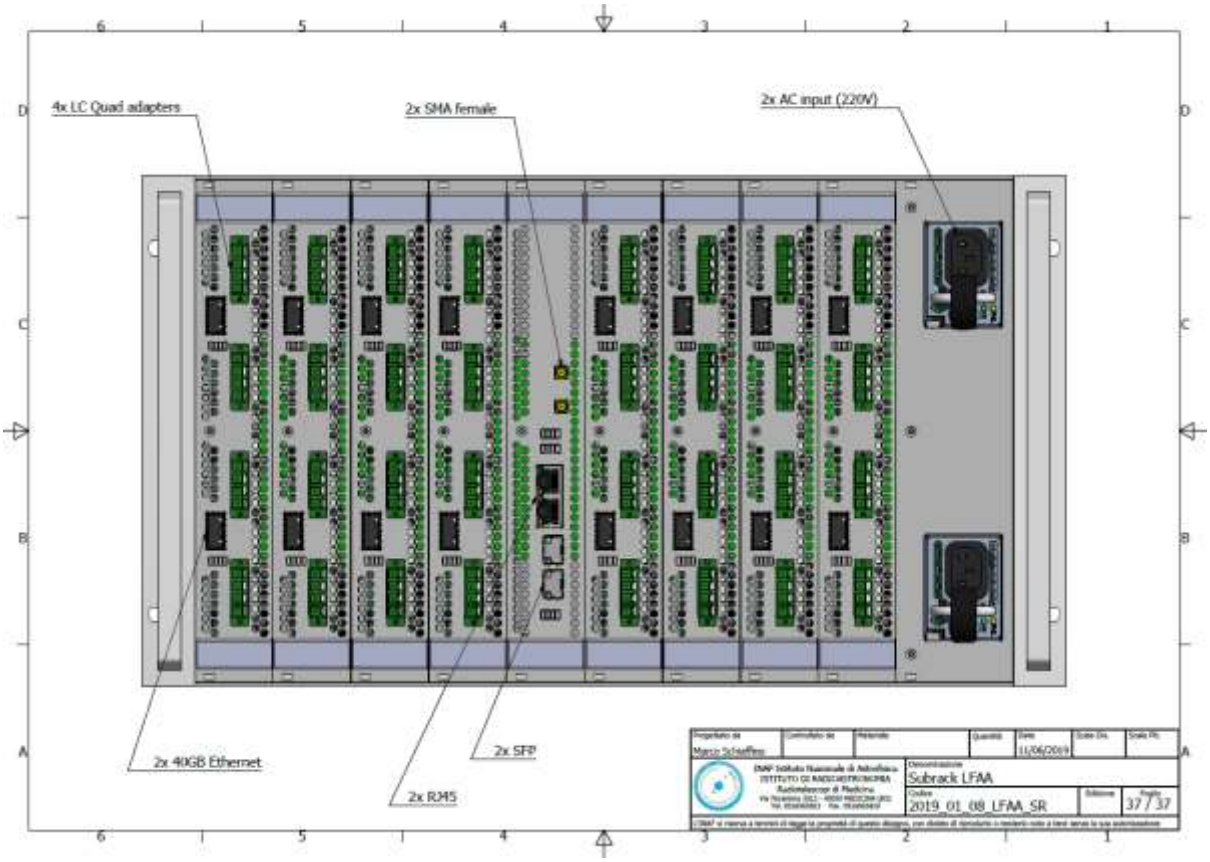


Figure 17 Front rear of the Subrack.

8 Tile Processing Module

The TPM is the main processing component within the SKA-LFAA element. It is a hybrid analogue/digital module that receives 32 analogue input signals coming from 16 dual polarization antennas (one SKA tile) via RFoF links and contributes with the cooperation of other tile processors to form the station beam. In fact, since each TPM computes the beam of one tile and sums the incoming partial beam from previous tile processors with the tile beam formed locally, when connecting more tile processors in a daisy chain the output of the last will be the beam of the station. The product breakdown structure of the TPM board is resumed in Figure 18.

The TPM is mainly composed of two boards: the ADU (Analogue to Digital Unit) board and pre-ADU boards. Pre-ADU boards are devoted to optical-electrical conversion, filtering, amplification and equalization of 32 analogue signals. The ADU board has the task of: analogue to digital conversion, polyphase filtering, application of calibration and beamforming coefficients, sum of all 32 signals to form the tile beam (local), sum the tile beam with the incoming partial station beam and transmission of the data to the network (switch).

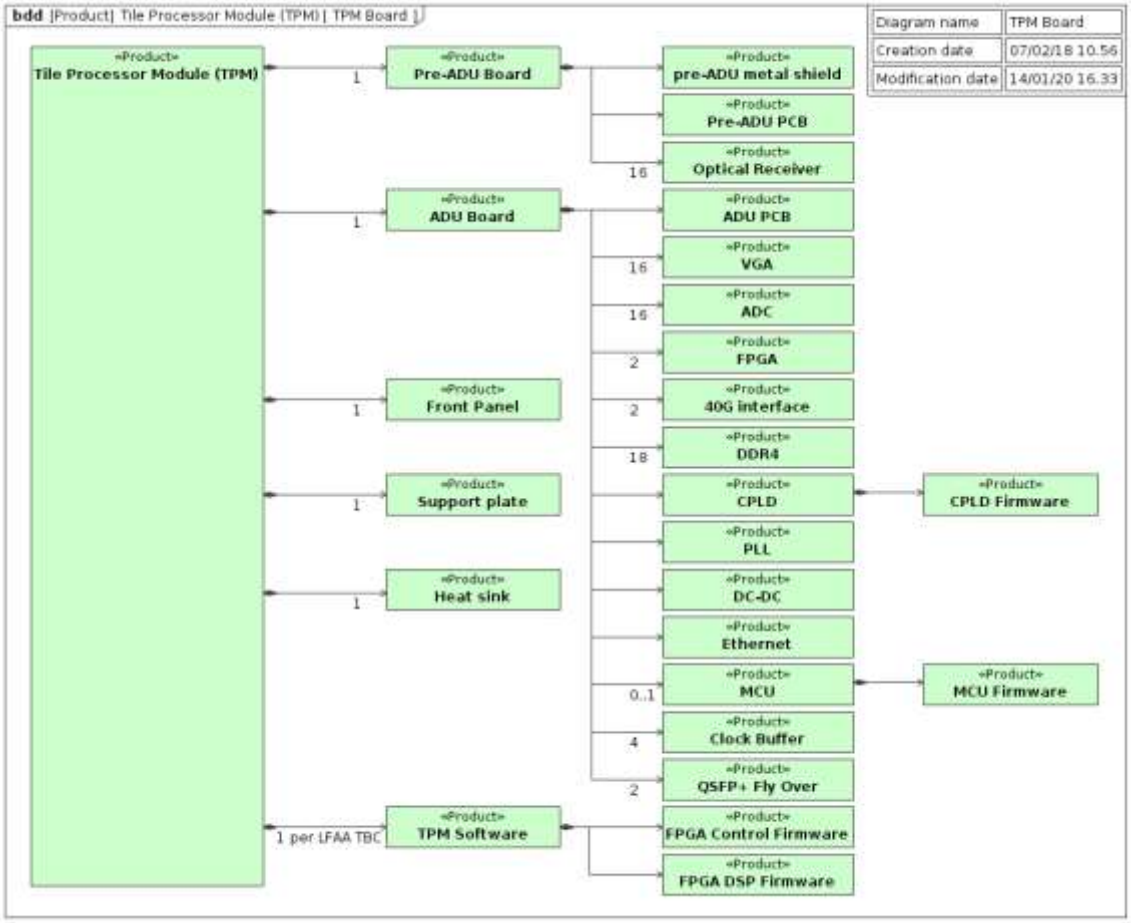


Figure 18 TPM - Product Breakdown Structure.

Several generations of the boards which constitute the TPM assembly have been designed and produced to verify the performances, the effectiveness of architecture but also used to develop the FW/SW necessary for FPGA processing and control functions of the board respectively.

The work in AAVS-1 was to de-risk this development as much as possible and optimise the design with industry participation. The version mentioned is the TPM 1.2 (assembly of ADU 1.2 & pre-ADU 2.1). A more integrated version was designed for LFAA and delivered to CDR (TPM 1.5) by INAF/Oxford in collaboration with Leonardo Finmeccanica, Sanitas EG and AAVID Thermalloy. The difference between the designs, in terms of integration, can be remarkably observed Figure 19. Dimensions and mechanics of the TPM 1.5 assembly are shown in Figure 20 and Figure 21 respectively.

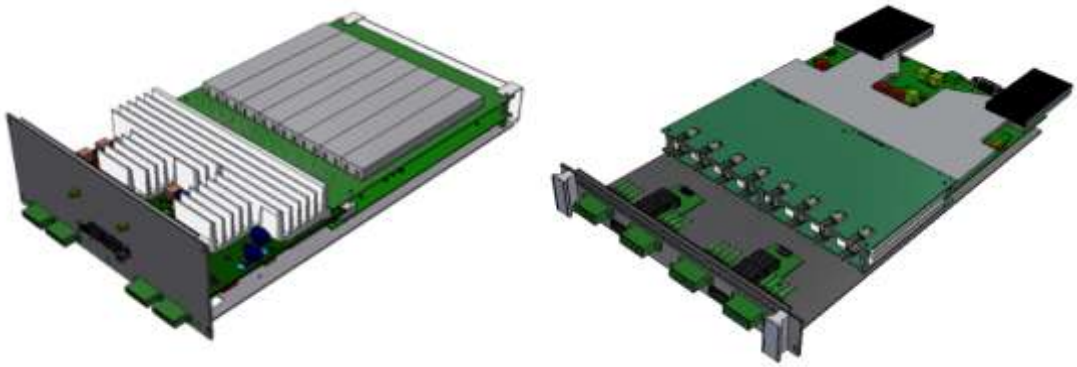


Figure 19 TPM 1.2 (AAVS1) vs TPM 1.5 (LFAA).

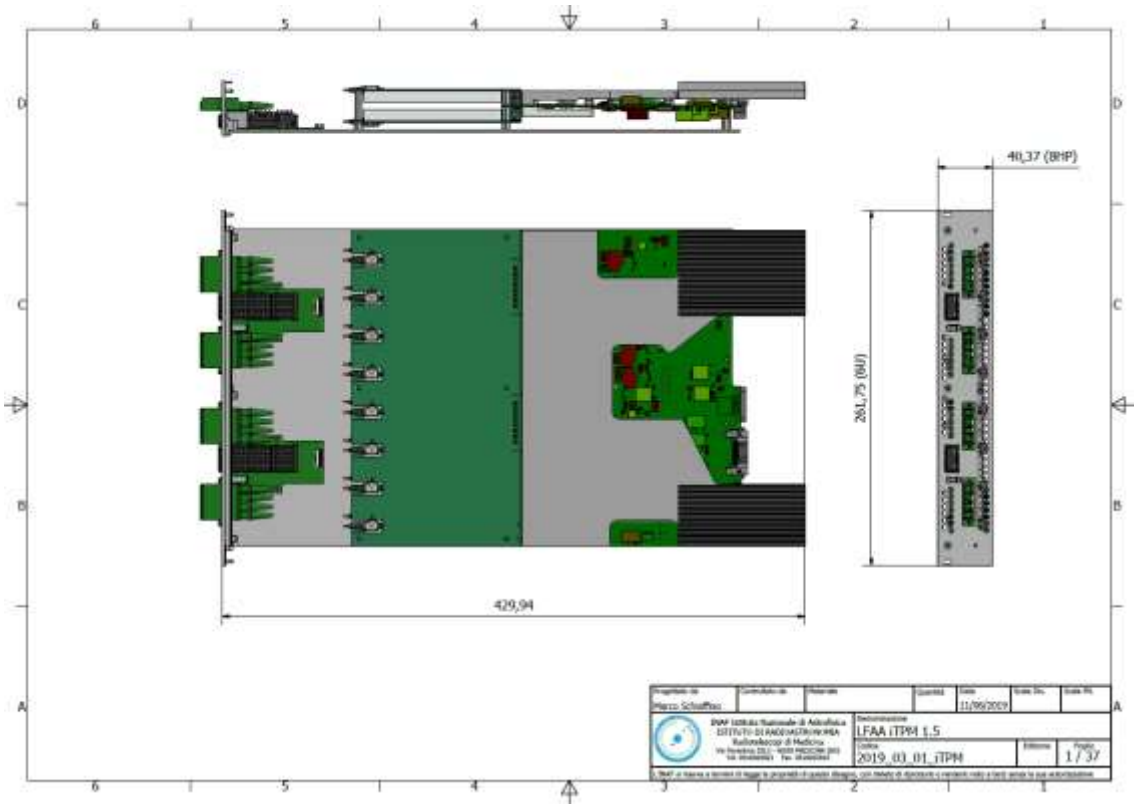


Figure 20 Dimensions of TPM 1.5.

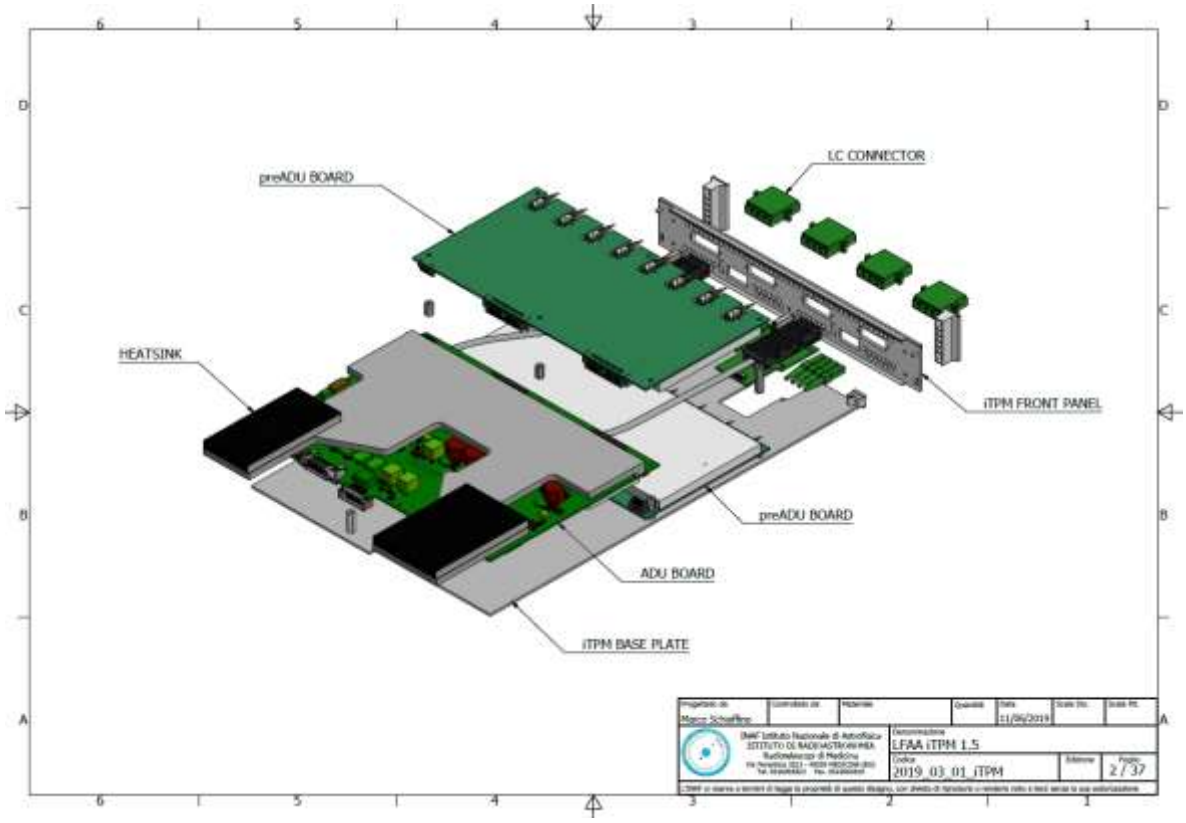


Figure 21 TPM 1.5 assembly.

8.1 Pre-ADU Board

Pre-ADU board corresponds to the analogue receiver in front of the ADU. The current design pre-ADU 2.1 hosts 8 double channel analogue receivers (i.e. 16 analogue chains). The two chains in each double channel receiver correspond to the two antenna polarizations.

The first stage of any pre-ADU channel is an optical receiver (ORX) which converts back to the RF domain the signal transmitted through an optical fibre from the remote antenna. The current pre-ADU version adopts WDM (Wavelength Division Multiplex) optical receivers, which paired with WDM optical RFoF transmitters at the antennas, allow to use one single fibre for both antenna polarizations.

A standard direct RF receiver (i.e. without any frequency conversion) follows the ORX. Several functions are here included to adapt the signal for the digital conversion: amplification, level adjustment (by means of a digital step attenuator, 31 dB range/1 dB step). The digital step attenuator is controlled by ADU board via the SPI bus.

Architecture of the pre-ADU board are reported in [PD7].

The design of this board is still progressing simplifying the mechanics and interconnection to ADU, but also the RF electronics. In particular, we would underline that the future generation will consider the possibility to use a differential driver stage in front of ADC (what we called VGA) and thus, it will allow us to avoid the last amplification stage and any digital control on board because the VGA is directly controlled by SPI.

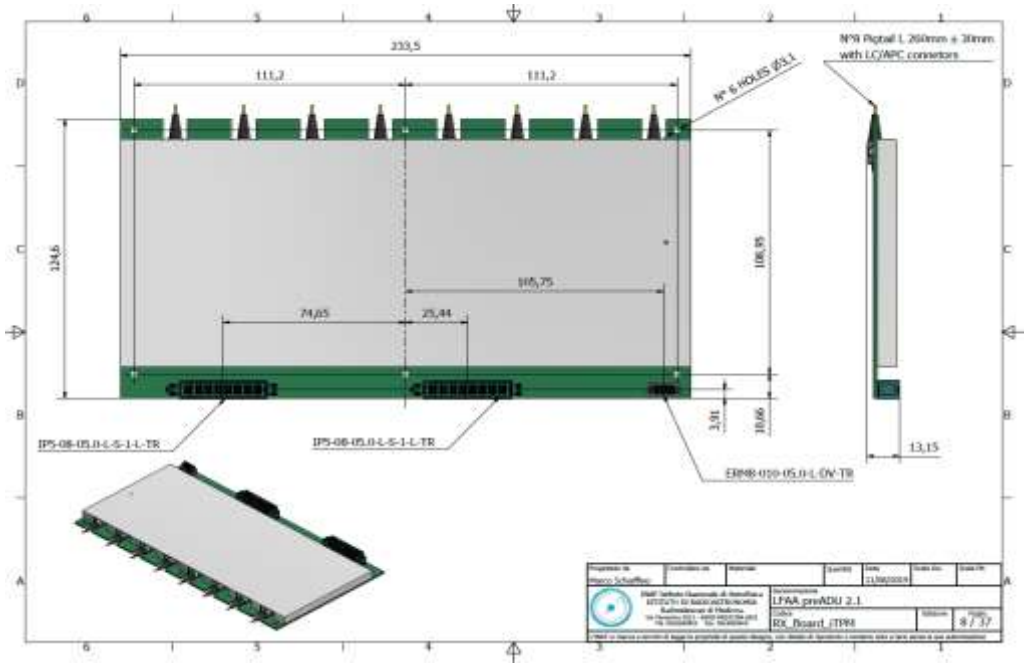


Figure 22 Image of Pre-ADU board prototype.



8.2 ADU Board

The ADU is the main hardware component of the TPM signal processing platform. It includes an analogue part, performing single ended to differential conversion of the antennas' RF signals, and a digital part, accomplishing high performance filtering and pre-processing of the acquired data.

It is a 6U board containing sixteen dual-inputs Analogue to Digital Converters (ADC) and two Field Programmable Gate Array (FPGA) devices, capable of digitizing 32 RF-paths and processing digitized input signals respectively.

The ADU project started in 2013 and various releases of the board have been implemented in the course of the years. ADU board generations are synthetically sketched in the next section.

8.2.1 ADU Board technical evolution

The component list and board architecture have been maintained through the successive implementations. Changes have been made as follows:

- ADU 1.0 first release. Main issue in under dimensioned input DC-DC supply and some component layout optimization needed for soldering process
- ADU 1.1. Initial DC-DCs were doubled, some minor bugs corrected, 32 data channel acquisition characterized. Product complete and stable
- ADU 1.2. Same BOM as 1.1 just some minor layout changes for ADC sampling clock equalization. ADU 1.1 and TPM-ADU 1.2 are firmware and software compatible
- ADU 1.5. Migration of the previous component list to the equivalent newer one, yielding 20% reduction of absorbed power and cost. The board architecture, in terms of component placement, clock distribution and board structure shares the same specification of the ADU 1.0 to 1.2

8.2.2 ADU Board main features

The ADU 1.5 was developed for the CDR. The rationale for this development has been a global effort towards power reduction. The main components of the ADU have been upgraded with respect to ADU 1.2. FPGAs have been replaced by Xilinx 16 nm Kintex Ultrascale+ devices; the AD9680 ADCs have been substituted by AD9695 ADCs; DDR3L memories have been updated to the DDR4 family to improve RAW data buffering. The board hosts sixteen memory chips, 4 Gbit each, with a 64-bit wide memory bus, for a total of 4+4 GByte memory.



Figure 23 ADU Board 1.5, without heat sink.

The following list sums up the main ADU R1.5 characteristics and features:

- Compact size, 6U format compatible
- Thirty-two analogue input capability with high quality and high isolation stackable RF 50 Ohm input connectors
- Sixteen dual channel analogue programmable drivers (amplifier/attenuator)
- Sixteen dual channel 14 bit 1Ghz AD9695 converters
- High quality clock distribution system with full JESD204B Subclass 1 capability on all inputs, with deterministic latency between the channels and the user configurable low noise PLL
- Two Xilinx Ultrascale+ XCKU9P 16 nm FPGA devices dedicated to data processing, pin to pin compatible, implementing the same functionality as the previous version
- Two DDR4, 64 bit memory banks, up to + 4+4 GByte total size
- Two 40G Ethernet interfaces (QSFP), one for each FPGA
- High speed internal bus to connect the 2 FPGAs, 40 Gbit + 40 Gbit bidirectional
- Low-level gigabit Ethernet management interface with instant ON flash-based Lattice CPLD
- Complete system monitor interface with power, voltage and temperature monitoring
- Two on board 256Mbit SPI user flash for multiple FPGA configuration options
- Second level management Microcontroller Unit (ARM Cortex M4, 32 bit, 120 MHz) for high level remote board control
- High efficiency multistage Power Distribution system, with configurable start up sequence and selective function related power control capability.

Thanks to this evolution, the ADU board still maintains the original architecture, increases the performance/resources while reducing of about 20% the absorbed power.

ADU 1.5 fits a 6U high and 170 mm depth standard rack mount format. Differently from the previous 1.2 release, the board is mounted with a backplane. As described in Section 3, this allows connecting and managing multiple TPMs with a subrack.

While the user connectors are grouped on one side, the RF inputs are on the opposite one. Several mounting holes are present for rack mounting and to fix a heat sink. An overview of the board mechanical layout top view is available in Figure 24.

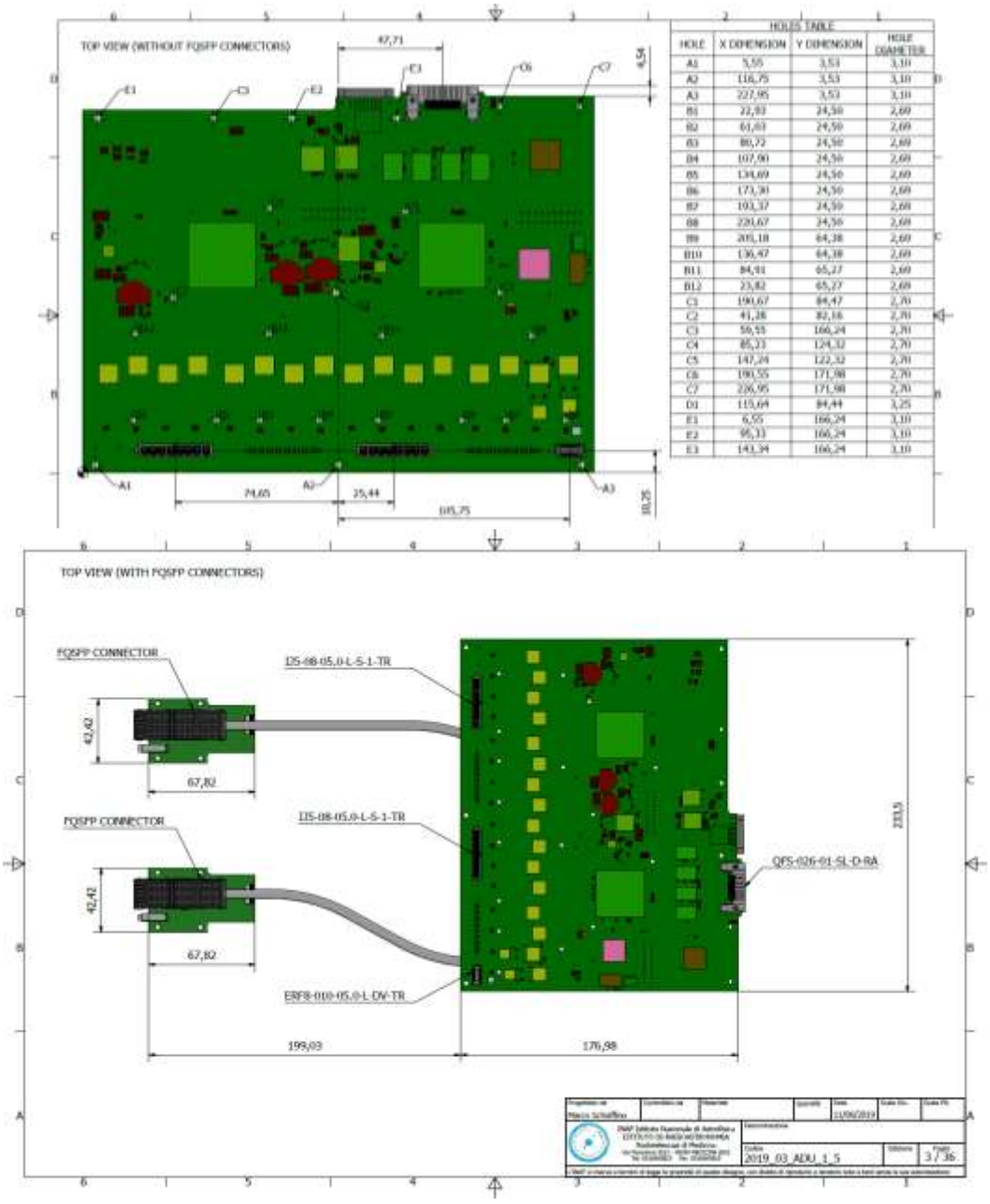


Figure 24 ADU 1.5 top level schematics. In the lower figure, FQFSP connectors are shown.

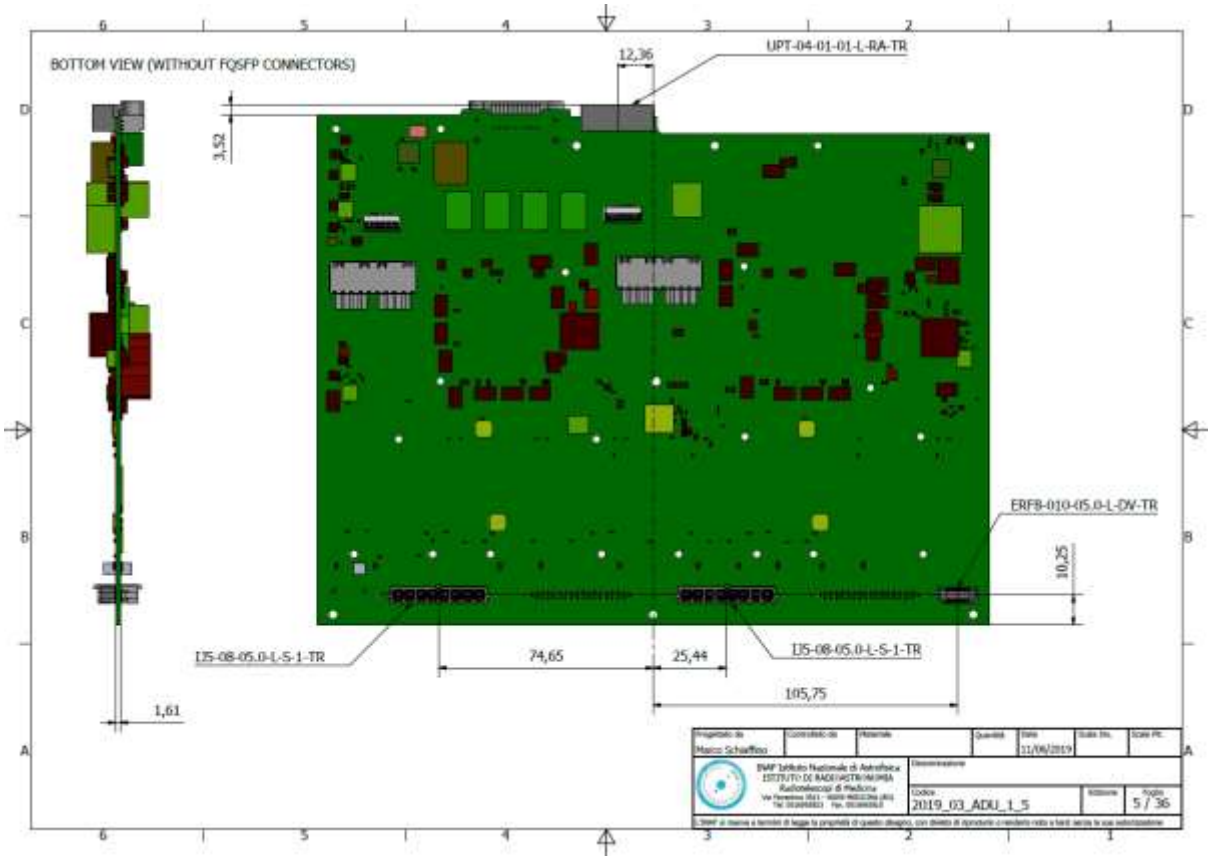


Figure 25 ADU 1.5 bottom level schematics.

All the relevant power-dissipating devices are placed on the top side to facilitate the design of a large heatpipe system required for the AD devices and the two FPGAs. Such a system has been described in Section 6.

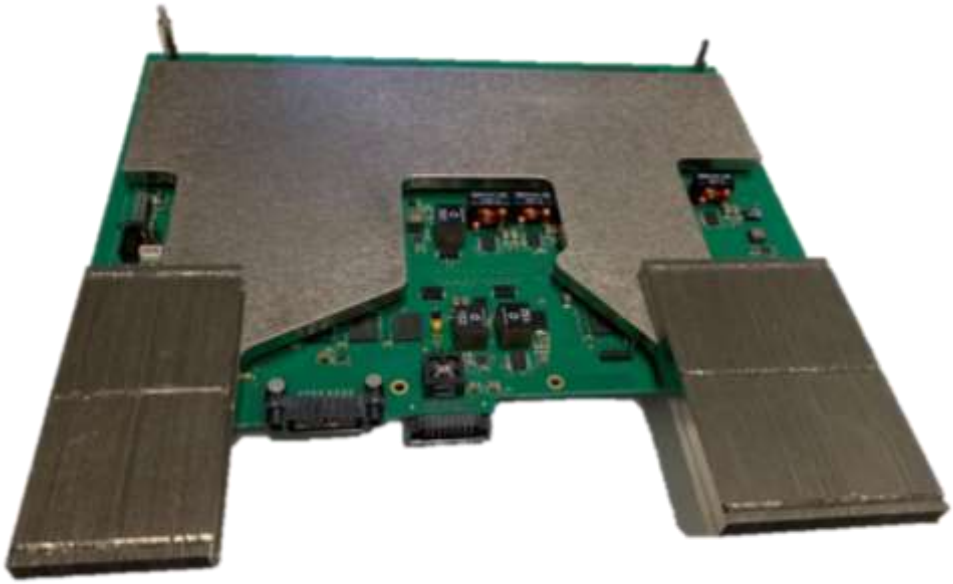


Figure 26 ADU Board 1.5 with heatpipe system mounted on it.

The heatpipe system requires adequate airflow in relation to ambient temperature and board power consumption. Main component and PCB temperature sensor available on the board shall be monitored to verify correct dissipation. Al the DC-DC converter and the AD converter are protected from internal maximum temperature.

The ADU board is organized in three areas, from left to right (Figure 25): management and power supply, FPGA and memories, analogue signal interface.

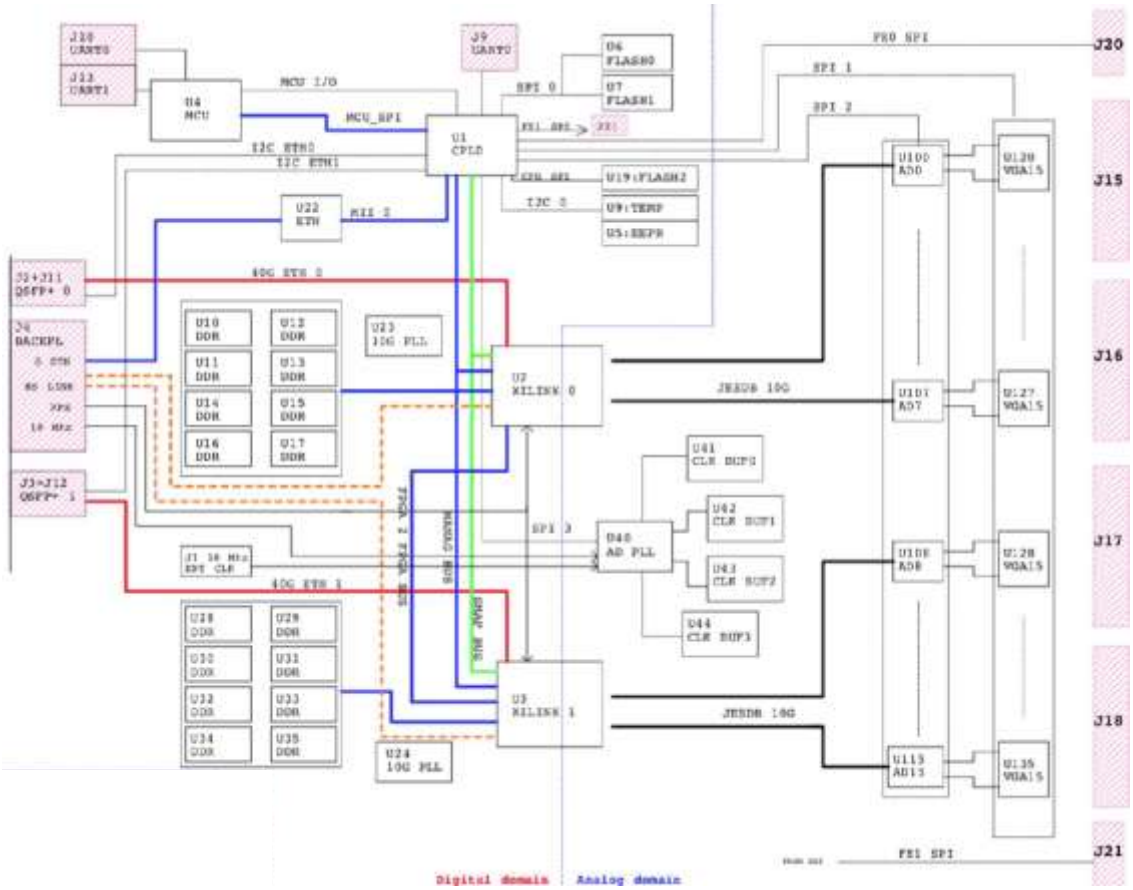


Figure 27 ADU Board Block Diagram.

The organization of physical components layout into three separate areas has been adopted to obtain performance and noise isolation between DC-DC converter, digital elements and analogue interface:

- The **management interface** includes the 10/100/1000 data link, the FLASH based CPLD (U1), the Micro Controller Unit & System Monitor (U4), the SPI FLASH memories (U6, U7) and the CPLD external configuration flash, U19.
- The **FPGAs** are two identical devices (U2, U3) that provide suitable and efficient resources to implement all the main board data management and elaboration. Each FPGA contribute to the System Monitor function.
- The **analogue section** includes the acquisition clock generation and distribution network (U40, U41 – U44), the sixteen dual channel ADCs (U100-U115), the thirty-two analogue buffers (U20-U135), the thirty-two baluns and the four RF high isolation x8 input connectors (J15-J18). Two connectors (J20 and J21) provide supply and digital SPI control for a pluggable analogue board for signal over-fibre connection and physical connection.

8.2.3 ADA and no ADA ADU versions

The analogue to digital conversion chain was developed in collaboration with Analog Devices Inc. for the first prototype release ADU 1.0 in 2014. A dual solution using ADC chip technologies ahead of commercial introduction (end of 2014) was evaluated: a passive matching network (without power



amplifier before ADC) and an active matching network (with power amplifier before ADC). The boards were manufactured using the same PCB, allowing the amplifiers to be bypassed through a matching network. This dual solution has been preserved trough the successive prototypal series.

The boards were named after the initial ADA4961 power amplifier employed for ADU 1.0: NO ADA in case of passive matching network, ADA in case of active matching is named ADA. The ADA4961 chip has been replaced by the ADL5202 VGA chip for the ADU 1.5.

The main advantage of employing NO ADA board is less amplification close to the digital lines, and thus less perturbations/noise. It also helps at saving cost and power. This is has been the low risk solution adopted so far.

However, in the future it might be considered making a release with the buffer amplifier, getting rids of the amplification on the pre-ADU board. Given the variable gain, the digital step attenuator on the pre-ADU board as well as its digital control part could be eliminated. In practice, the pre-ADU would have no control elements.

9 Subrack Management Board (SMB)

The SPS management unit integrates the TPM service functions required at rack and subrack level with high-level command interface with the telescope manager application.

The management board is actually instantiated in two possible configurations, rack and subrack with combined functions.

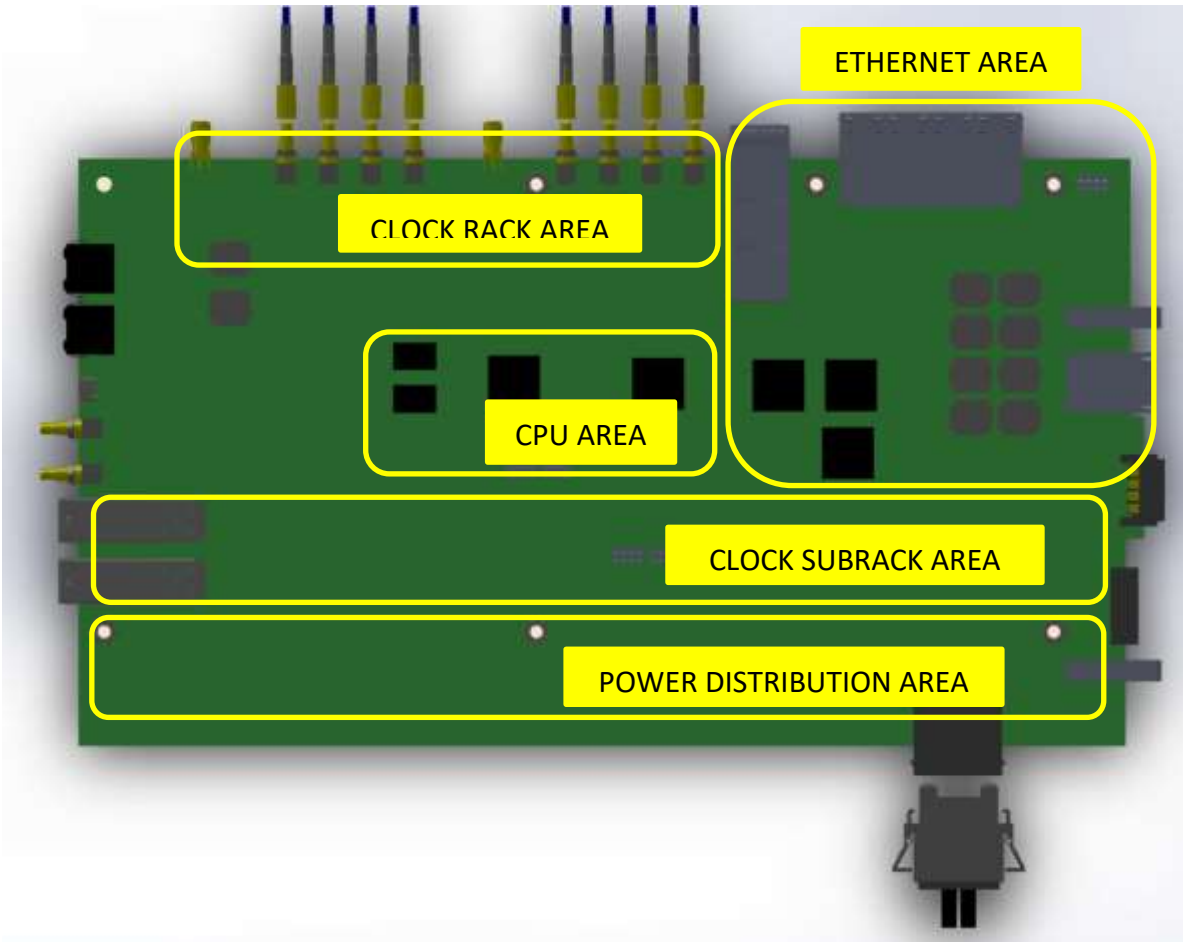


Figure 28 Management Board top placement and layout guidelines.

In the rack configuration the management board is boxed in a 1U drawer to provide the following main functions:

- Interfaces with the SKA 40G Ethernet network
- Provides the rack level 1G local Ethernet Network
- Interfaces with the SKA 10 MHz & PPS Rack synchronization signals and distribute them in the Rack
- Provides a Linux-based CPU to execute high level rack function
- Interfaces all rack elements for remote control operation and monitoring.



In the subrack configuration, the management board is plugged in the backplane to provide the following main functions:

- Interface the rack Ethernet network to TPMs
- Distribute or regenerate the synchronization signal to all TPMs
- Manage and monitor subrack power supply and power distribution to all TPMs in the subrack
- Manage and power the FANs for the Sub-Rack air cooling system
- Provide a Linux-based CPU to execute high level subrack functions
- Provide the Ethernet network interface for the remote field station.

The following list sums up management characteristics and features:

- 6U size format compatible, 350 mm depth
- Single supply, 12 to 24V DC input
- 1x4 high quality 10Mhz clock distribution (differential)
- 1x4 PPS distribution (single ended)
- Digital PLL high quality 10Mhz re-generation and jitter cleaning function
- One 40G Ethernet interface (QSFP) with only one 10G Ethernet active
- Up to 18 port Gigabit Ethernet Switch with 10G Uplink
- Low-level gigabit Ethernet management interface with instant ON flash-based Lattice CPLD
- High performance ARM9 based CPU, dual core running @ 1Ghz with enhanced capabilities
- Solid state 4GByte FLASH system memory, for OS and data
- Four DDR3L, 64-bit memory banks, 1 GByte total size running @ 1Ghz
- SD card slot for FLASH memory expansion
- Two USB 2.0 and HDMI output for additional User Interface
- CPU trace port available on a high-speed connector for SW debugging
- Complete system monitor CPU with power, voltage and temperature monitoring
- 256Mbit SPI user FLASH
- Two I2C board temperature sensors
- Two EEPROM for board configuration data with pre-assigned MAC address
- Expansion GPIO connector with UART, CAN, SPI, I2C, PWM available functions
- SATA II interface connector for hard disk storage capabilities
- 1x PCI Express interface for expansion capabilities
- Interface for external battery pack.

A picture of the SMB is shown in Figure 29.



Figure 29 Subrack Management Board.

9.1 Mechanical overview and board layout

Management board fits a 6U high and 350 mm depth rack mount format, compatible with TPM defined layout.

An overview of the mechanics of the Subrack Management Board is shown in Figure 28 and Figure 29.

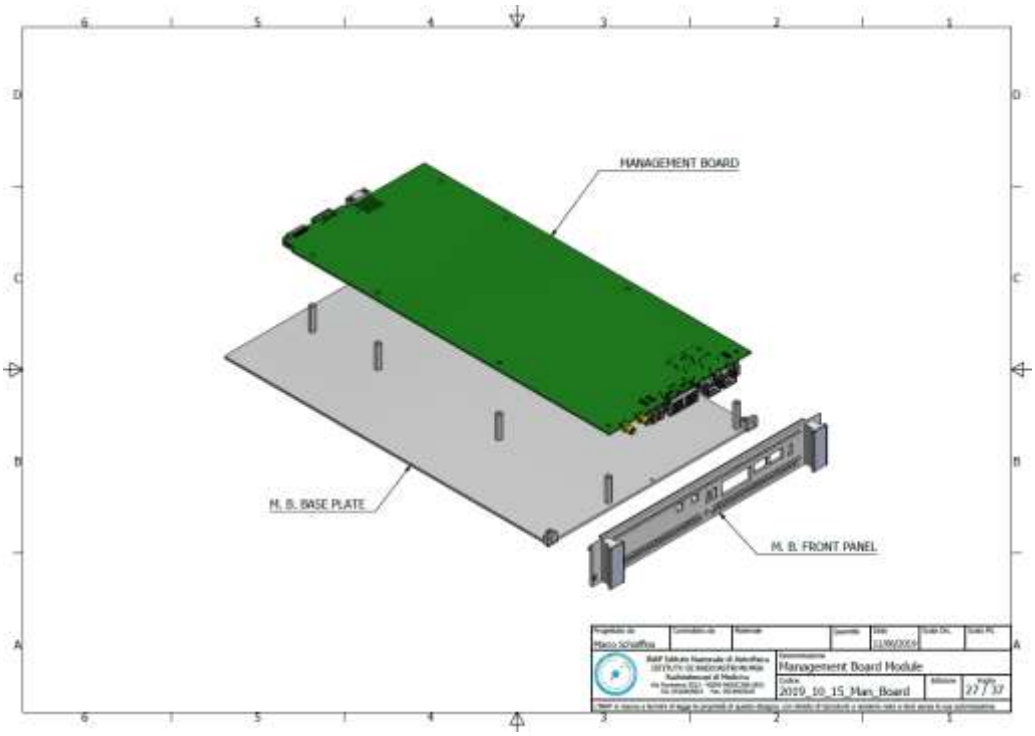


Figure 30 Dimensions of the Subrack Management Board.

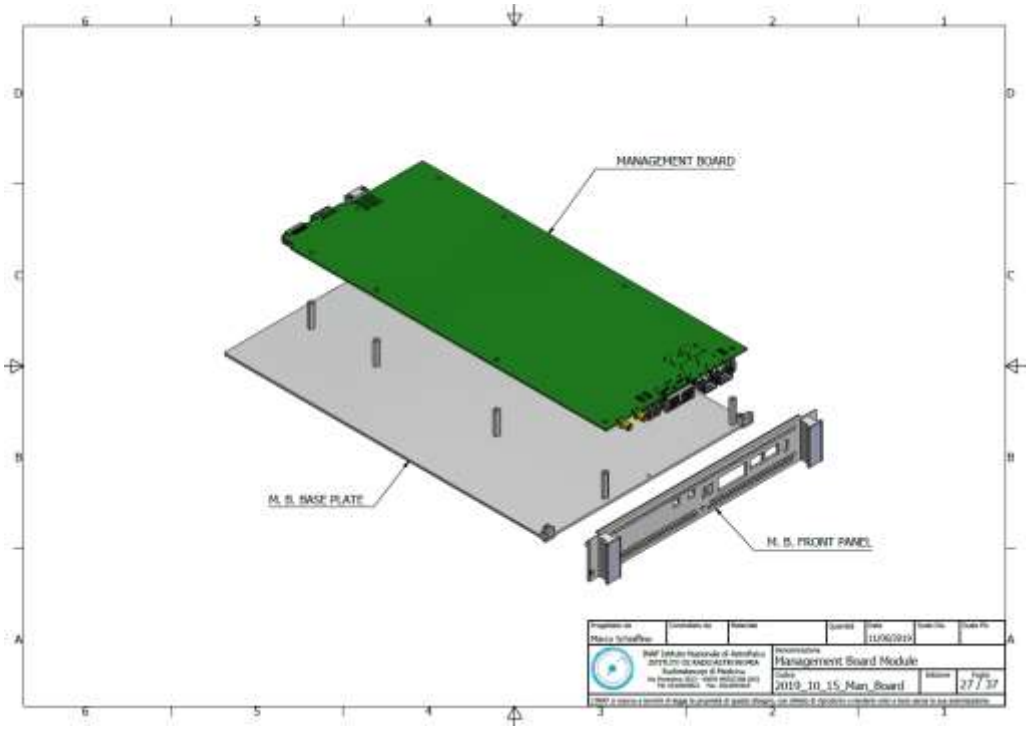


Figure 31 Base plate and front panel of the Subrack Management Board.

The board is designed to avoid active dissipation in a controlled temperature environment. In the 1U drawer and in the backplane a low speed air circulation shall be enough for heat sink dissipation.

In the bottom side only, low profile components are present without significant power consumption.

Board layout is organised with function specialized areas for optimal layout and performances.

The clock areas are considered RF circuit and separated from the possibly noise sources high speed digital circuits, with the same approach successfully adopted on the TPM board.

The overall generous board size (233x350 mm) allows optimal placement and component separation, for dissipation and isolation issues.

For the clock layout, the bottom side will be preferred for all RF critical devices.

All the digital circuits, excluding some low power memories, are placed on the top side to simplify the board assembly and testing.

9.2 Management block diagram and main functions

A block diagram of the management board is shown in Figure 32.

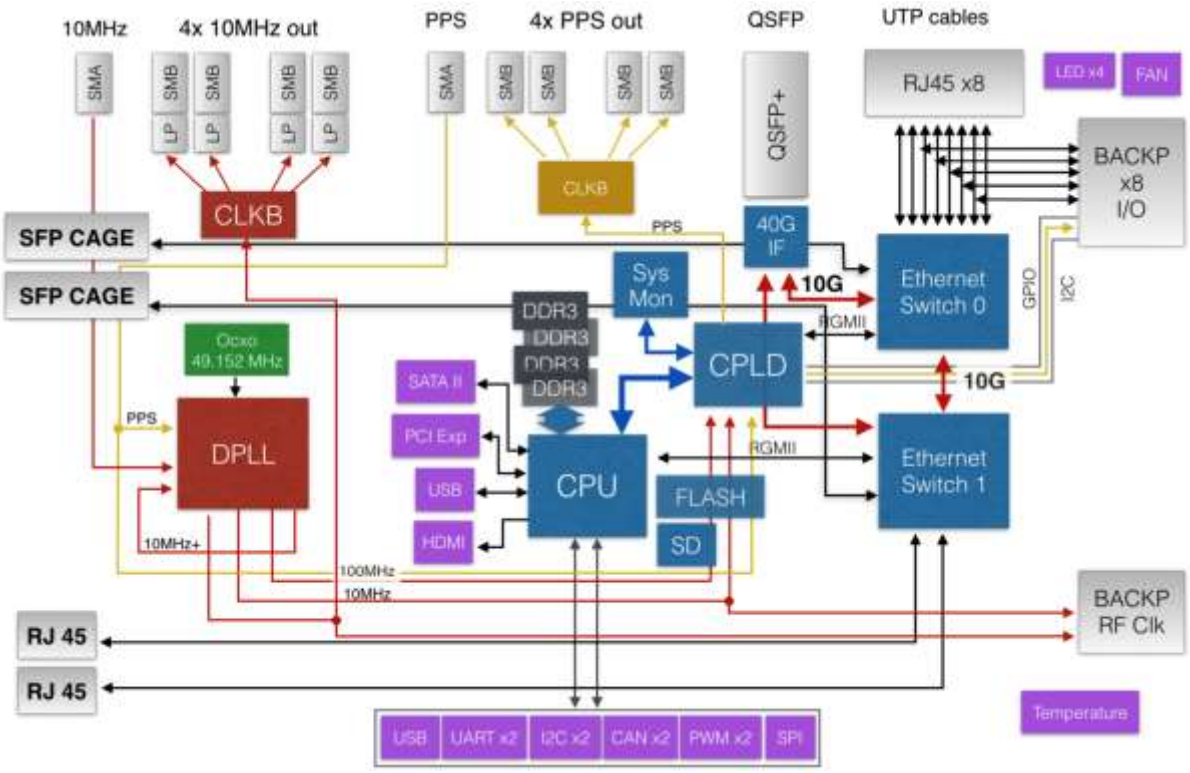


Figure 32 Management block diagram.

The Management processor board is organized in three areas, from left to right: clock & PPS distribution, CPU and monitoring function and Ethernet function.

The organization of physical components layout into three separate areas has been adopted to obtain performance and noise isolation between DC-DC converter, digital elements and analogue interface.

The clock & PPS distribution includes the differential x4 RF clock buffer (U38, U41), the Digital PLL (U42) the digital clock buffer (U39) and a selection of 49.152 MHz high quality system clock sources.

This clock circuit has been updated based on the clock distribution feasibility study for LFAA cabinet, selecting the previous active mode for the 10 MHz distribution and a hybrid passive mode for the PPS distribution.

The previously proposed PPS ENCODE function has been dismissed because of the DPLL functional limitation that doesn't allow to manage the phase relationship of the ENCODED signal and the PPS input signal.

The final design will implement the **active** 10 MHz clock distribution circuit, with the optimal Jitter removal, and the passive PPS distribution, with the capability to measure and manage the phase relation between the incoming 10 MHz reference and PPS signal.

In the **active mode**, the digital PLL is used to regenerate the 10 MHz reference clock removing the high frequency noise components from the input reference signal. A low pass digital filter is enabled on the input and only the phase reference information is maintained in the generated output.

This feature allows better performances on the clock distribution and no dependencies from the incoming clock reference signal high frequency noise or high frequency signal components.

Thanks to that, the high frequency component of the 10MHz signal distributed from the management to the subracks inside the cabinet will be removed with a Low Pass Filter on the signal source side, greatly reducing the possible electromagnetic emission from the required cables.

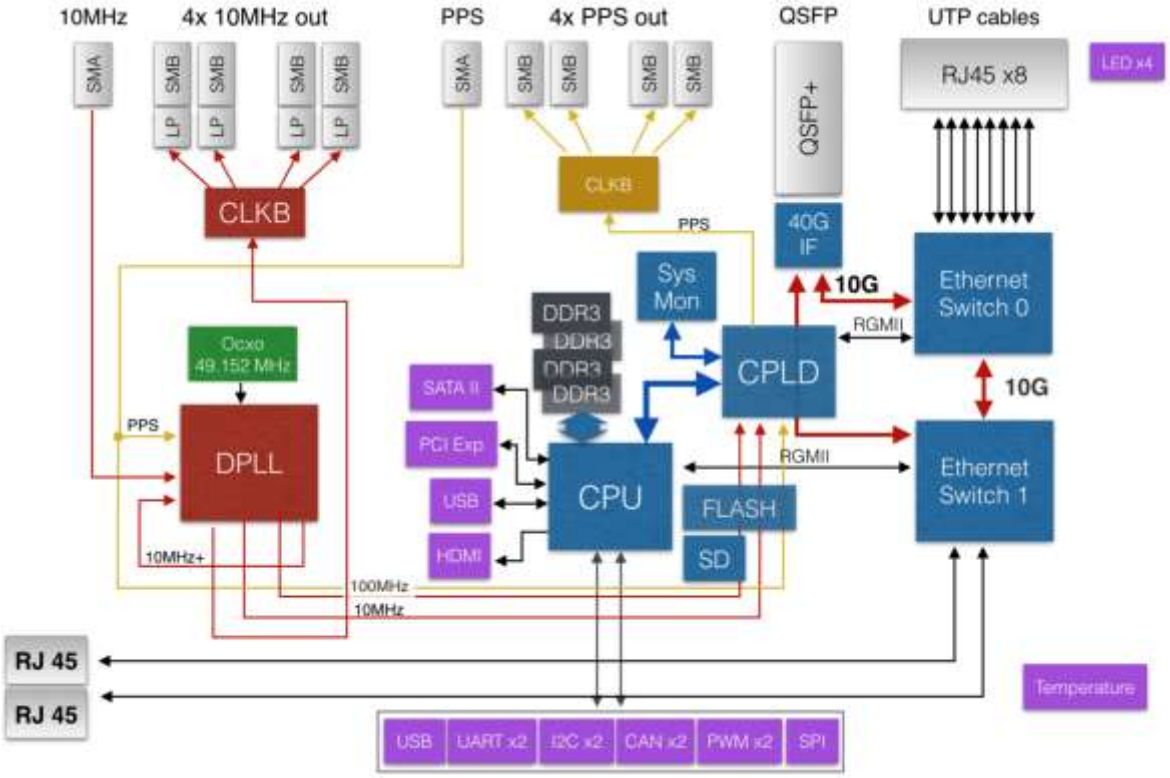


Figure 33 Cabinet management clock configuration.

In the cabinet configuration the incoming 10 MHz reference signal is connected to the DPLL, input A to generate a phase aligned 10 MHz and 100 MHz outputs. These signals are also connected to the CPLD and will be used to allow a rough measurement of the PPS input phase. One 10 MHz low jitter is routed to the 4x CLOCK BUFFER output that generates 4 synchronous signals, one for each subrack. Before the clock output connector, a low pass filter removes the high frequency component of the signal.

The PPS signal is connected to the DPLL, input B_p and directly to the CPLD. Another 10 MHz output signal (in phase with the input reference) is routed back to the DPLL input B_n to execute a precise phase offset (time difference) measurement between the PPS edge and the 10 MHz reference closest edge.

The CPLD receives the PPS and shall perform a programmable delay line to change the PPS output phase that is distributed to the subracks with the dedicated clock buffer.

The measurement of the time difference between the 10 MHz reference and PPS signal at the beginning of the acquisition and possibly adjust the PPS phase is crucial, to avoid possible PPS Jumps

around a 10 MHz rising edge in the calibration and signal acquisition phase and allow a stable acquisition.

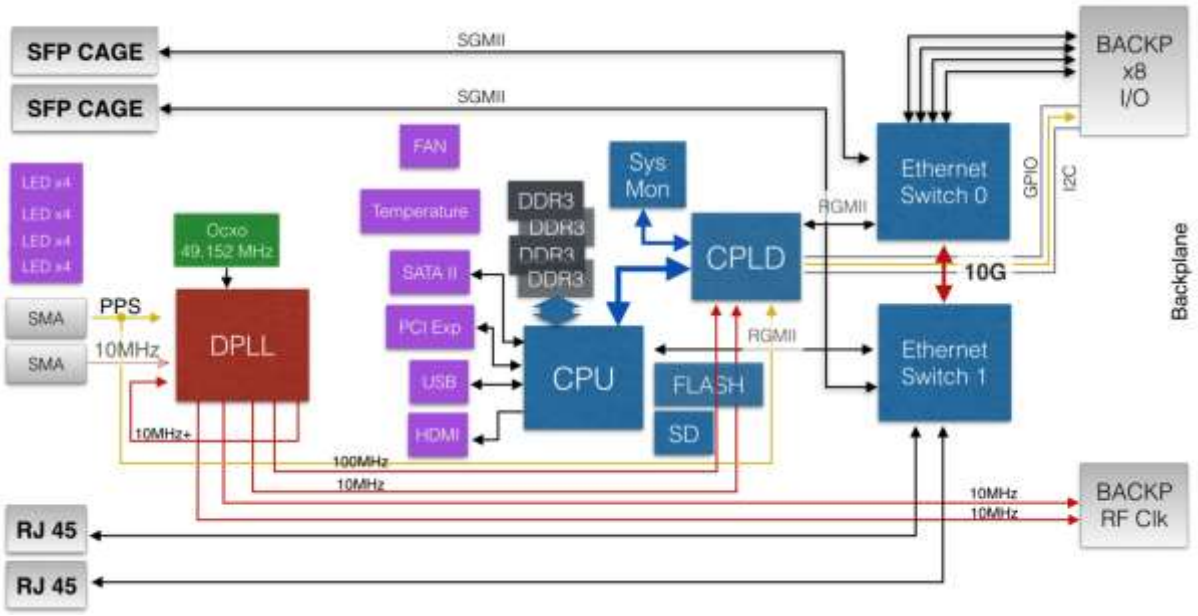


Figure 34 Subrack management clock configuration.

In the SMB, the clock configuration is similar but the generated 10 MHz by the DPLL are two and routed directly to the backplane.

The PPS generated by the CPLD is routed to the backplane with two signals through the high-density backplane I/O connector.

The Ethernet functions are distributed on three main devices: two identical multiport switches (U4, U5) and an optical 40G QSFP interface (U6). Each switch is connected to the other and to the optical QSFP interface with a 10G Xaui interface to create an 18 port gigabit switch with two 10G uplink channels. This architecture guarantees a 10G packet transmission capability from the board to the external network and this configuration is suited to support the Cabinet functionality. Connection diagram is in Figure 35.

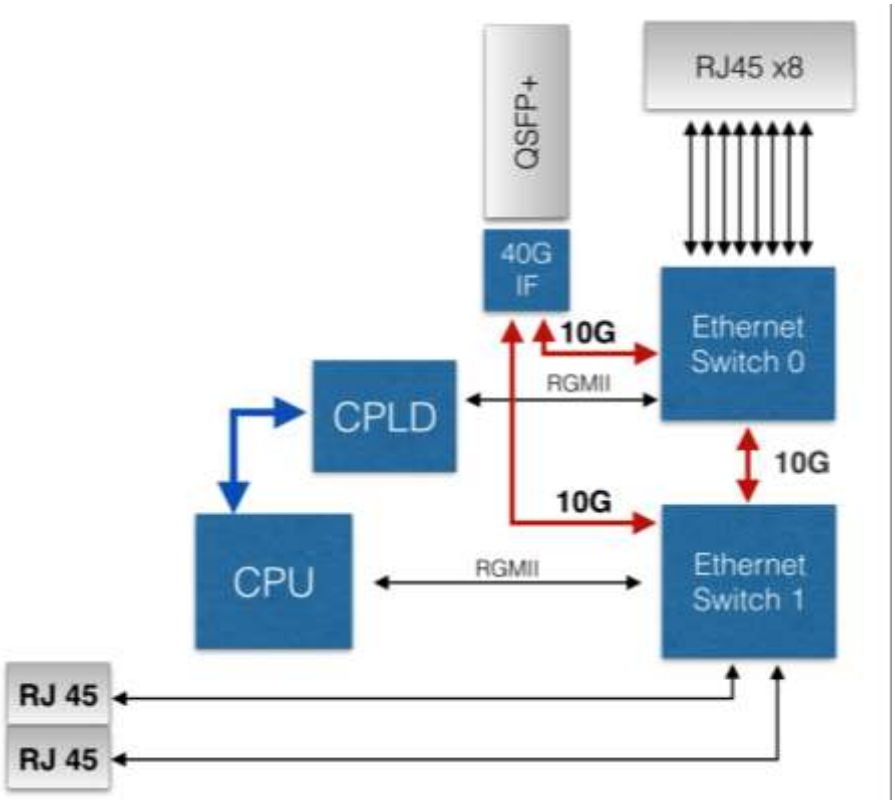


Figure 35 SKA Management Ethernet network, cabinet configuration.

The cabinet management network also provides 8 copper interfaces on the front panel and two copper interfaces on the rear panel to implement the required cabinet management network (RIF DDD).

In the subrack configuration (Figure 34), the 40G optical interface is not required and the related 10G connections to the switch are reconfigured to implement a single SGMII gigabit link to the SFP cage to add two Gigabit optical fibre interfaces requested for the field node electronics related to the antennas connected to the subrack itself.

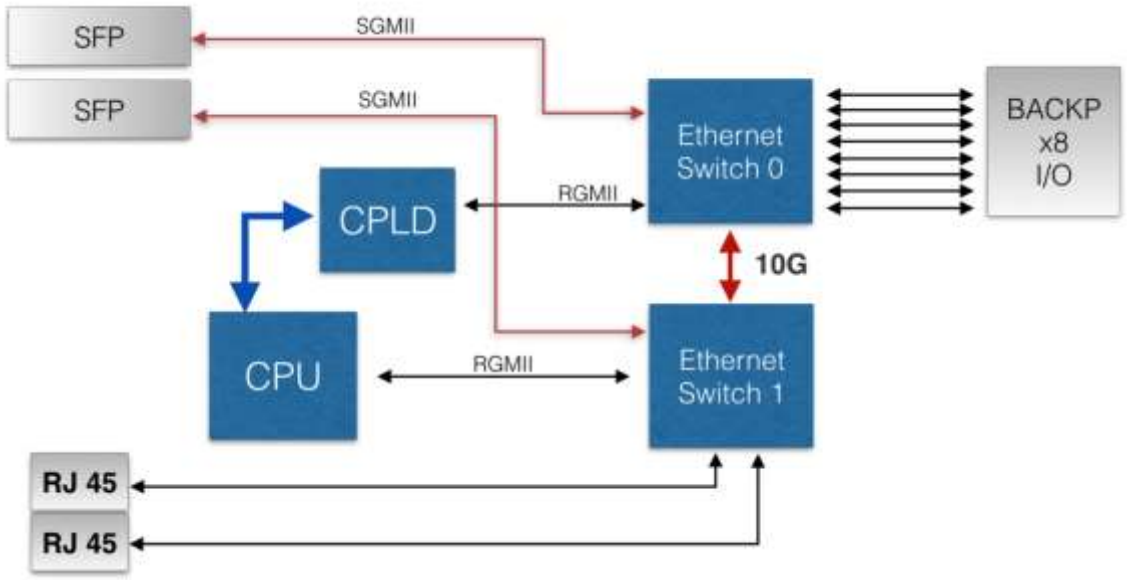


Figure 36 SKA Management Ethernet network, subrack configuration.

In the subrack configuration, the 8 copper interface of the Switch 0 is connected to the backplane high density I/O connector to reach the TPM gigabit interface related to the management network.

The two copper interfaces of the Switch 1 are available on the front panel to be connected to the cabinet management gigabit network.

The **CPU and monitoring** functions are distributed on three main devices: CPLD (U2), microcontroller (U3) and the main processor (U1).

The CPLD is connected directly to the management network and can implement a low level communication with all the critical system function to ensure system safety.

The microcontroller provides the Analog to Digital interface to measure internal voltages and control some accessories, like fans. The microcontroller is connected by an 8bit data, 14 bit address, memory bus to the CPLD.

The main processor is connected directly to the management network too and also to the CPLD with a memory bus interface. FLASH memories are available (U24, U36) for system boot and data storage. The processor is a dual core Arm9 architecture with several features (Floating point units, Graphical processing Unit, large cache and internal ram memory) and is completed by an external DDR3L memory bank (64 bit wide, 1GByte total capacity) running at frequency up to 533 MHz. For debugging and generic user interface two USB ports and an HDMI video output complete interface are available too.

The CPU SATA II interface is available on a disk-cable connector.The CPU PCIe interface is available also on a high-speed expansion connector for board capability expansion.

With this architecture the board can provide two IP address, for low level access to the CPLD or high-level command interface to the CPU.

10 Backplane

The backplane is sited on the back of the subrack chassis and provides each TPM with power and services required for LFAA operations. Only RF Fibres and 40G Ethernet are directly connected to each TPM from the front panel. A block diagram of the backplane is shown in Figure 37.

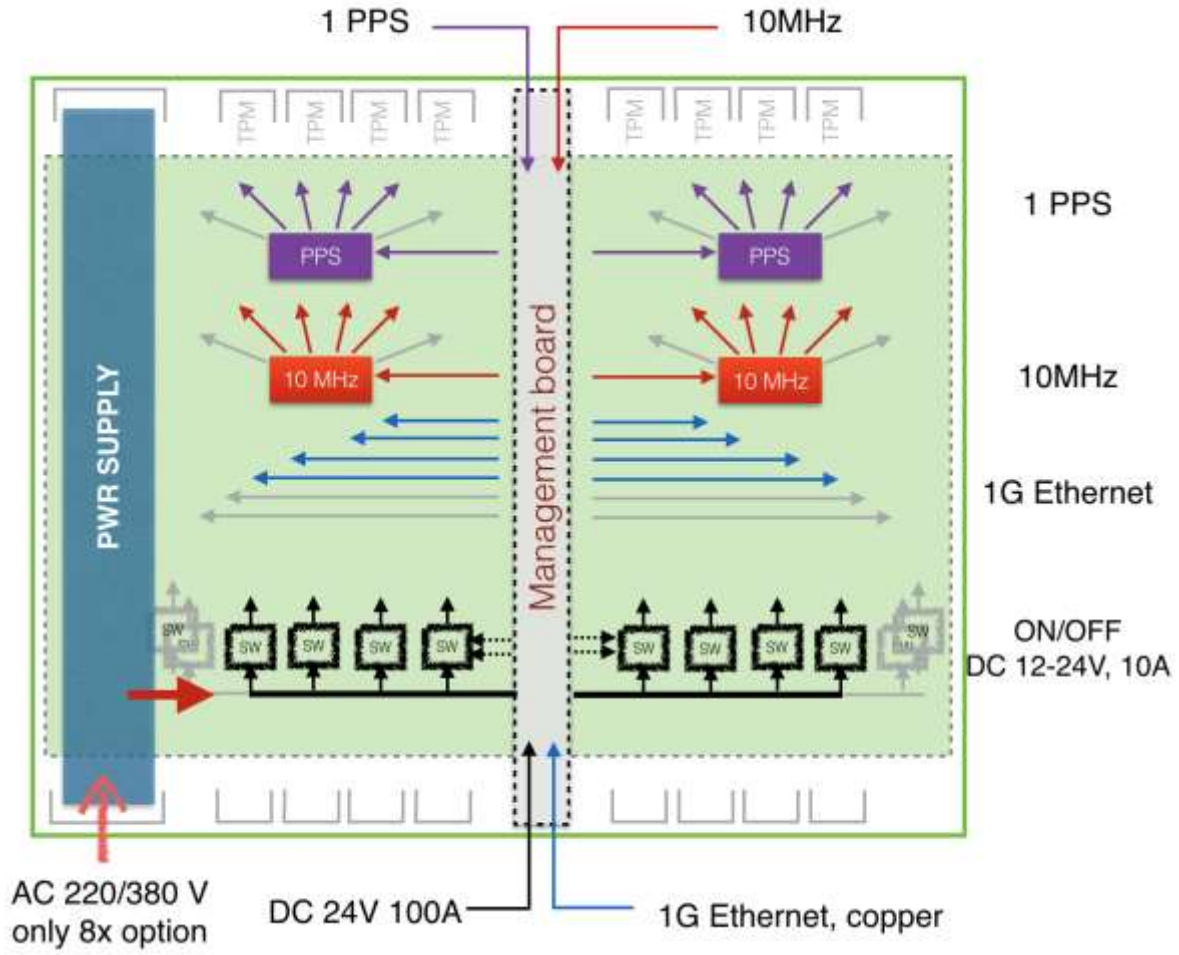


Figure 37 Subrack backplane block diagram.

The backplane provides mechanical interface and temperature measurement in two different points and the following functions:

- 8 slots for the TPMs, 1 slot for the SMB
- 1 a slot for Power Supply inserted in the subrack with a power connector sized to supply the whole subrack
- Detect the presence of the TPMs
- Distribute the PPS from the SMB to each TPM (Two single ended signal coming from the board shall be distributed to the TPMs)
- Distribute the two 10MHz clock to each TPM with low RMS jitter. One clock from management shall be distributed to 4 or 6 TPMs with differential interface

- The PPS and Clock signal shall be equalized and length matched between them and between each TPM
- Distribute the Gigabit Ethernet to each TPM (4 differential traces, 100 ohm matched for each TPM)
- Distribute the DC power to each TPM, measure the absorbed current, feature ON/OFF function sourced from the management or the local Power supply
- Monitor continuously power loading from each TPM and perform automatic switch-OFF in case of extra-current
- Interface to 4 FANs with speed control and limitation of absorbed power/speed
- Two serial bus, I2C and One Wire bus, to all TPMs for system configuration services
- Measure temperature in two different point of the board.

Backplane board specification:

- MHz RMS jitter contribution < 200 fs (tbc) with low insertion loss path
- 10 MHz isolation (vs all other signals) > 60 dB
- Power connector shall be capable to supply each TPM with 10A of maximum current
- Mechanical size shall be about 480x160 mm for the 8x version
- The PCB mechanical shall be designed in accordance with the subrack mechanical specification that will be delivered by INAF
- The layout shall guarantee very low DC resistance for the power distribution bus from source to TPM, maximum 1 mOhm/m.

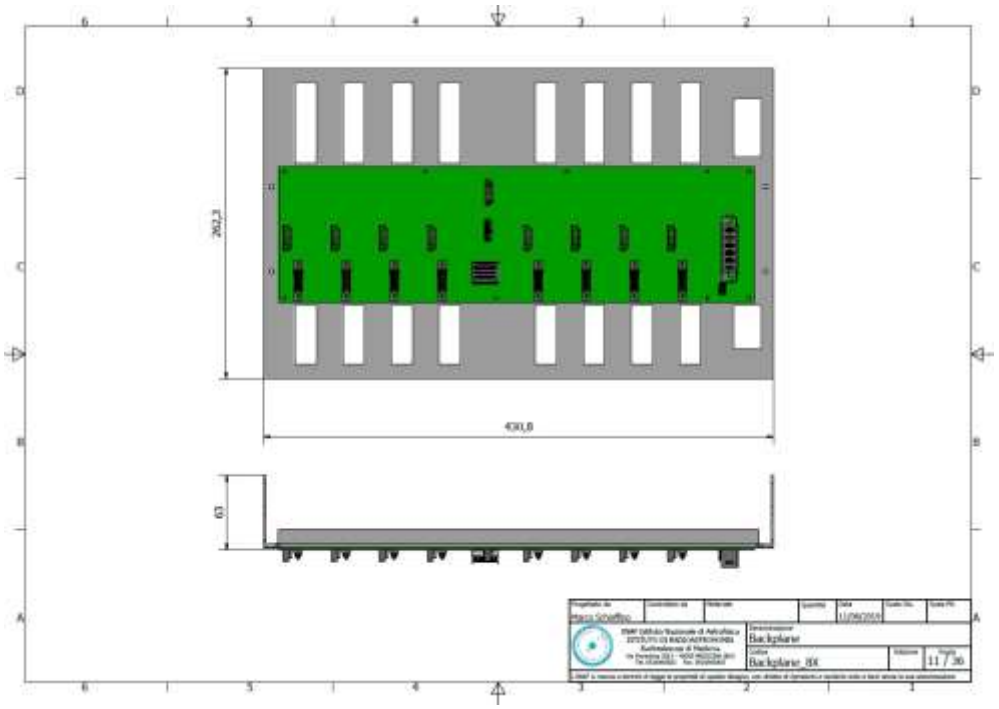


Figure 38 Dimensions of the Backplane.

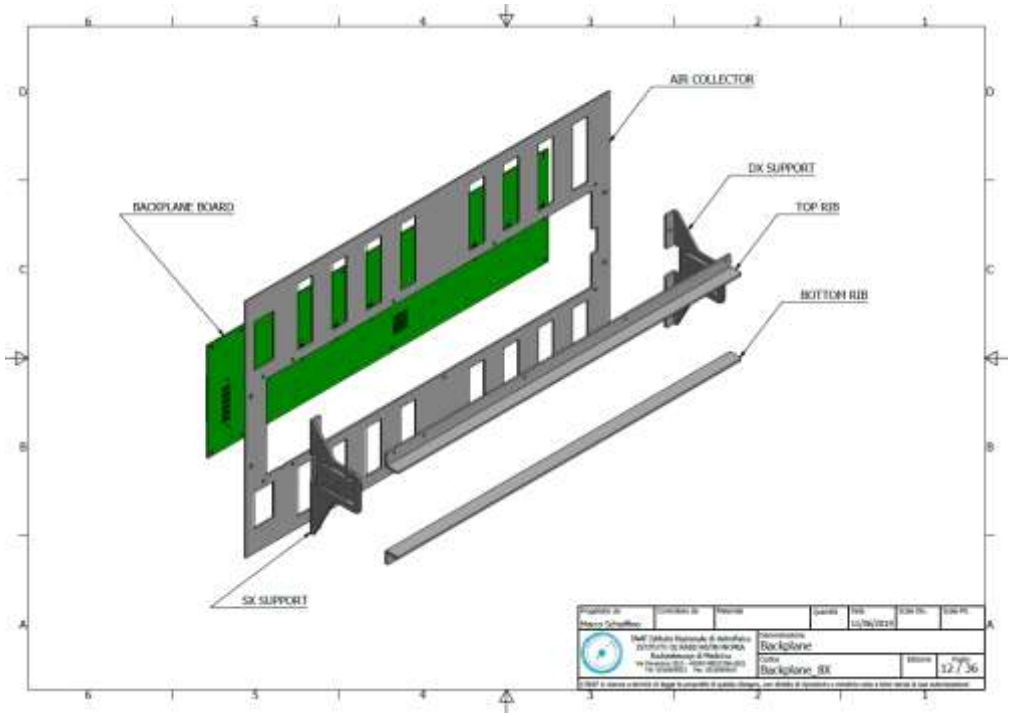


Figure 39 Backplane supports.

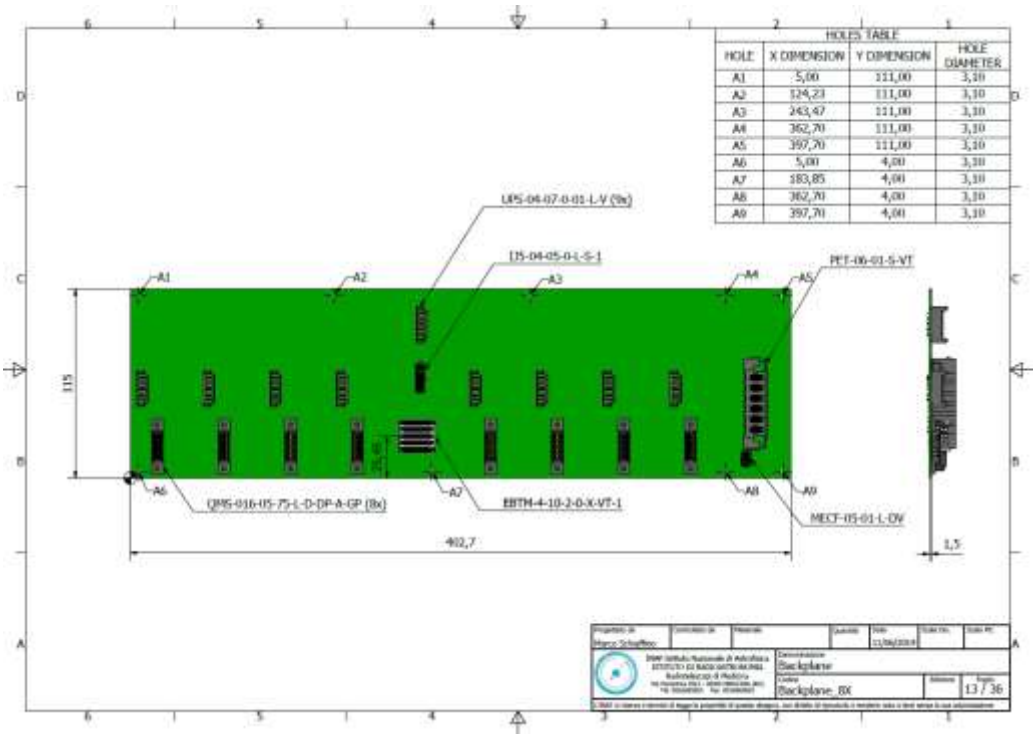


Figure 40 Backplane connectors.

11 Power Supply

As said in Section 3, SPS is physically implemented in 256 cabinets and each cabinet hosts 32 TPMs. The 32 TPMs are organised in the four subracks that also integrate the management boards. Each subrack is designed with two commercial redundant single AC phase power supplies [PS1] with 12V DC output joined together in the backplane [PD4]. These two devices are capable of 1300 Watt each, 108 A, with maximum efficiency of 94% at half load. A schematic diagram of subrack power unit is shown in Figure 39.

In normal condition, they work together at about 40% of their maximum capacity, close to the efficiency peak. In case of single failure, the load can be raised to 80% without functional limitation.

Phase unbalance may occur only if one sub-rack power module is active.

These power supply modules are remotely managed by the subrack management board and several parameters can be monitored [PS1].

The 12V output of each module is connected to the subrack backplane where the power is distributed to the subrack management board (always on) and to each TPM. Each TPM is switched ON and OFF by a specific Hot Swap IC that can also, monitor the absorbed current [PD4] and implement an automatic ON-OFF switch if the absorbed current overseas a programmable threshold.



Figure 41 Subrack power unit.

Preliminary subrack power allocation has been defined based on the following table:

Table III Preliminary power budget.

SUB-rack	Single Unit absorbed Power, Watt			Cabinet absorbed Power, Watt		
Element	**Load**	**Typical**	**Maximum**	**Number**	**Typical**	**Maximum**
TPM 1.5 (*1)	DC 12	107,8	120	8	862	960
Sub-rack Management	DC 12	22	30	1	22	30
Sub-rack backplane	DC 12	5	5	1	5	5
Sub-rack FAN (*2)	DC 12	20	50	4	80	200
Power Supply, off 94%	AC220V	29,5	34,5	2	59	69
TOT LOAD, AC:					**1028**	**1264**

*1 The TPM absorbed power if greatly application dependent and shall be fixed only upon final application release

*2 Subrack Fan implement an adaptive speed control, the absorbed power will change upon external air temperature and TPM absorbed power

The power supply module has been selected from the commercial devices and Joined with the subrack by a mechanical and interface board to the backplane.

The identified modules have a standard size and connectors and are available from several companies with a variety of characteristic with power upon 2000W.

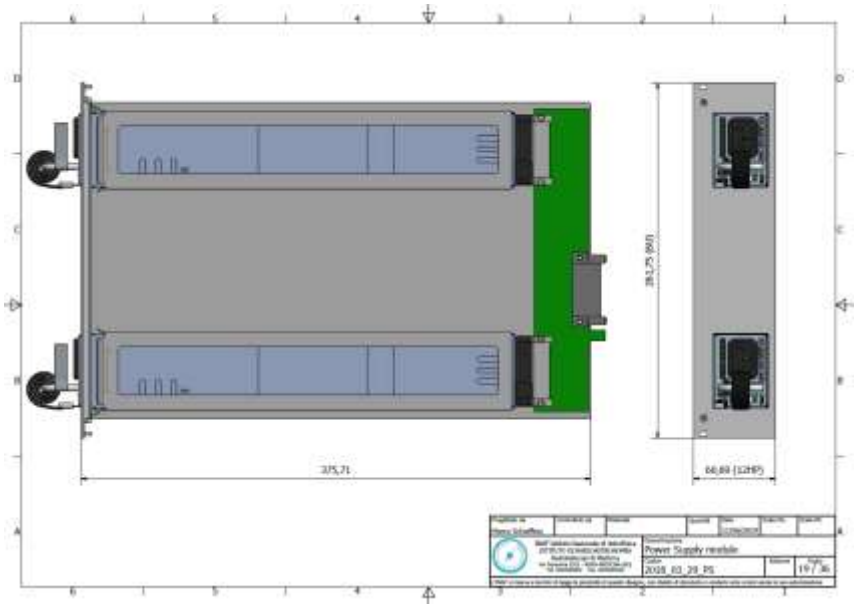


Figure 42 Integration of the Power Supply unit in the Subrack.

The Power supply units can be removed and replaced for maintenance from the front panel. Each Power Unit is remotely controlled and monitored by the subrack with a serial bus available through the backplane.

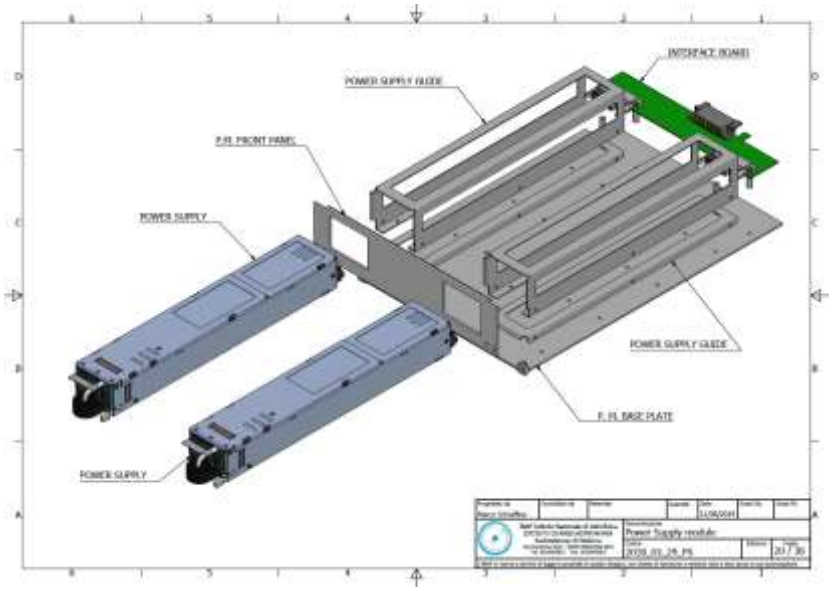


Figure 43 Power Supply unit supports and guides.

Only qualified supply power units can be used and appropriate device driver shall be selected by the subrack management software.

12 Monitoring and control

Subrack monitor and control function execute the main following functions:

- Monitor all the main supplies in critical point, voltages and currents
- Power ON/OFF several structured elements
- Execute pre-defined Power ON and Power OFF sequences
- Monitor temperatures.
- Monitor clock distribution PLL status
- Monitor alarms and warnings
- Manages subrack internal air flow speeds

Monitor and control function are implemented and executed at TPM level, by the on-board MCU, and at subrack level for low level function by the MCU and at functional level by the CPU.

All these element communicate by the gigabit management network and by interrupt lines for high priority events.

Safety function are implemented locally to minimize damages.

Subrack monitor and control supply and sensors scheme can be summarized in the following figure:

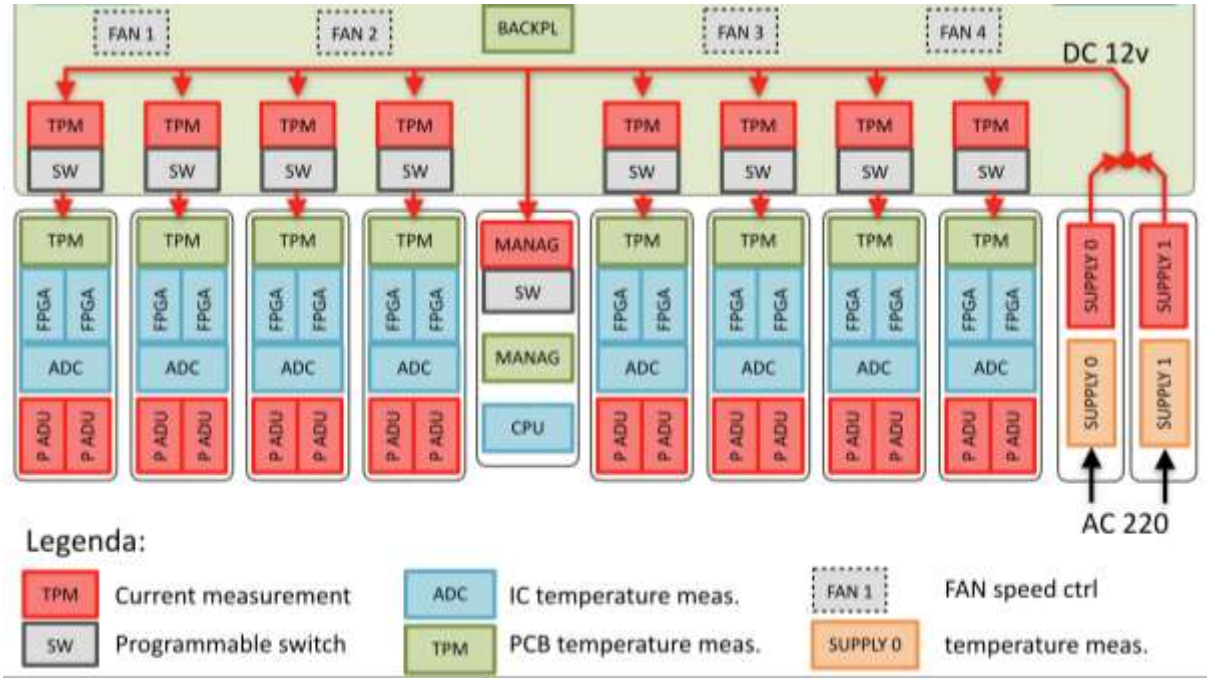


Figure 44 Subrack monitor, control supply and sensors scheme.

The current measurements is done at three levels:

- Supply output, embedded in commercial modules, 2 measurement points
- Management supply Input, associated with a safety programmable switch

- TPM supply input, associated with a safety programmable switch, 8 measurement points.
- TPM pre-ADU supply input, 32 measurement points.

A total of 43 current measurement are available, 9 of them with automatic safety switch off function.

The sub-rack voltage monitoring scheme is the following:

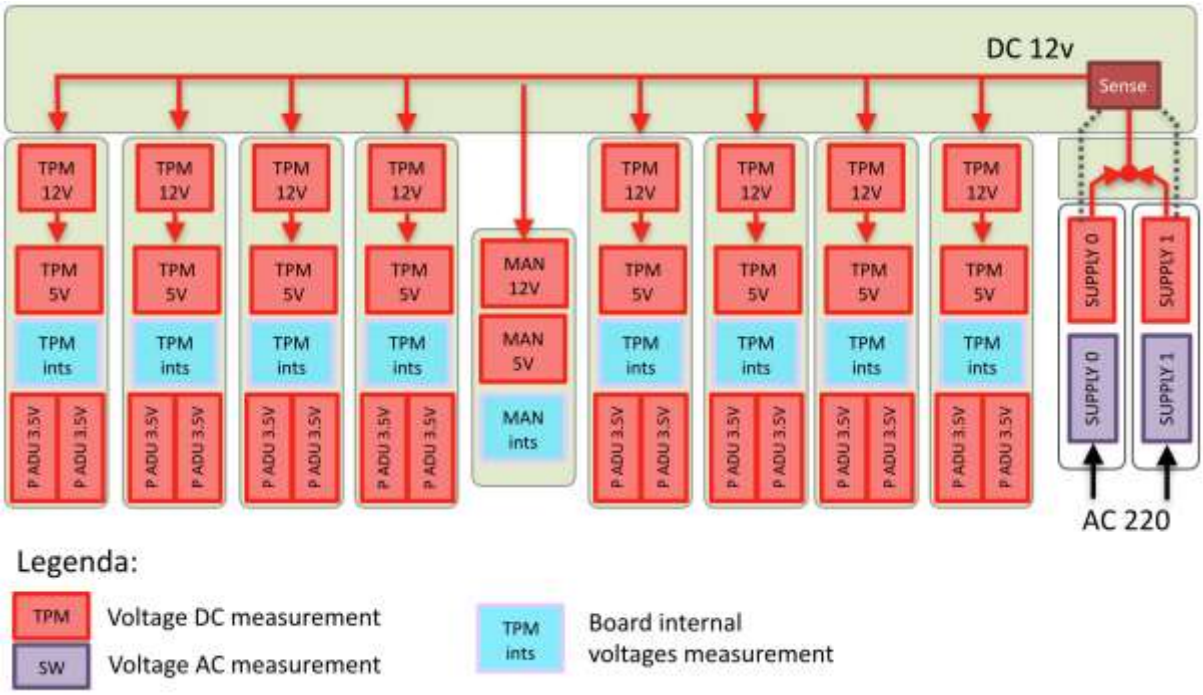


Figure 45 Subrack voltage monitoring scheme.

The following measurement points have been provided at Subrack level:

- AC input
- Power supply DC output
- Voltage sense on the backplane, one for each power supply modules
- Input voltage on the management board
- Input voltage on each TPM

These measurement point are integrated with the one available on each TPM and on the management board

The following temperatures are collected at sub-rack level in order to check system stability and provide information to the cooling system:

- TPM PCB base temperature (component free area)
- TPM FPGA core temperature
- TPM ADC centre temperature (place in the worst case PCB point)
- Backplane PCB base temperature (component free area)
- Management PCB base temperature (component free area)



- Management CPU temperature
- Power supply input temperature.

The subrack fans are controlled separately to provide differentiated air speed to compensate possible temperature differences inside the subrack.

The normal operative conditions shall be identified for all temperatures and a power/temperature monitor application shall run on the local sub-rack management board, and report the current values, possible warning and errors to the upper level application. The sub-rack management board shall signal the TPM status on the front panel LEDs, changing colour or with blinking, to drive manual maintenance.

The input power supply modules are remotely monitored and controlled to check input voltage level, output voltage level, internal temperature, internal fan speed and other power quality information.



13 SPS Subrack Timing Synchronisation

A study has been accomplished after the CDR to analyse the SPS synchronization distribution network, given the absence of a specific requirement for the clock to be provided in input to the cabinet [PD2].

Time and frequency for SKA1_Low is generated centrally and distributed to the LFAA Signal Processing Sub-system by the SaDT (SAT) (see [PD9]). Frequency reference is distributed as a 10 MHz sinusoidal tone, and time as a PPS square wave. There is not a fixed phase relationship between these two signals. PPS is referred to UTC. An NTP server in the network provides UTC time with an accuracy of better than 100 ms and typically 10 ms, sufficient to uniquely identify each PPS pulse and to properly synchronise LFAA and CSP.

In each SPS cabinet, a management board regenerates the frequency and time reference signals and distributes them, using coaxial cables, to individual SPS sub-racks. Subrack management board in turn distributes the signals to the subrack backplane, to individual tile processing boards. A phase-locked loop (PLL) in each TPM board generates the 800 MHz sampling clock, a 200 MHz synchronisation clock and a 100 MHz signal processing clock from the distributed 10 MHz. The proposed SPS subrack synchronization distribution network is detailed in Figure 46.

It was agreed to implement a twofold configuration of clock distribution for further analyses and evaluations:

- High quality differential passive distribution
- Active distribution with clock re-generation and jitter cleaning.

Preliminary tests have been accomplished using the active distribution system with a high quality 10 MHz reference input. The clock distribution tree has a measured phase noise of -148 dBc in the frequency range between 3 kHz and 10 MHz. Below 1 kHz, the PLL adds about 2.5 ps of jitter up to a few seconds.

ADC clock is derived using an Analogue Device AD9528 PLL, which specifies a clock jitter of -161 dBC/Hz above 10 kHz, corresponding to a jitter between 10 kHz and 800 MHz of 70 fs. Below 10 kHz it copies the input clock jitter. ADC itself has an internal clock jitter of 55 fs RMS.

The internal time labelling of the samples is determined using the PPS signal. This signal is captured in the FPGA, using a 100 MHz clock derived from the 10 MHz reference. Synchronisation is performed once at the beginning of an observation session, and the internal PPS is used for all internal timing. In this way it is guaranteed that there is always the same number of samples between PPS edges. Cycle ambiguity is avoided by measuring the phase offset between the PPS signal and the sampling clock, and choosing an appropriate phase for the resampling clock, where the PPS signal is stable. The mechanism has been tested in AAVS1 and proved to generate a repeatable synchronisation over more than 1000 power cycles.

Accurate measurement of the relative phase between the 10 MHz and PPS signals is also performed inside the DPLL in the cabinet and subrack management boards.

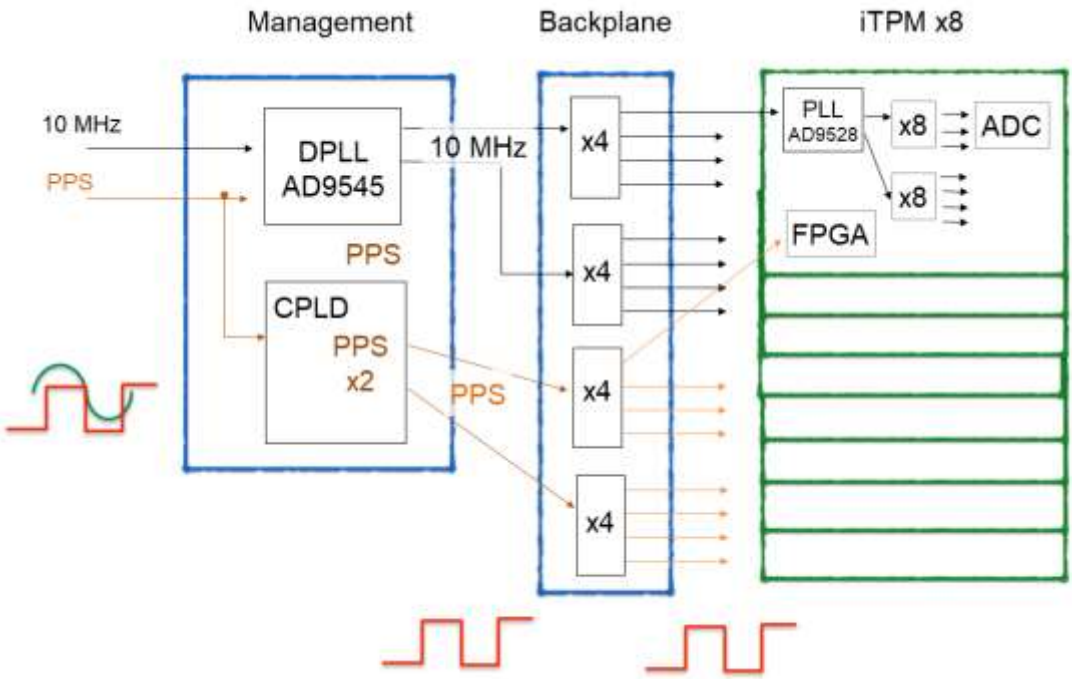


Figure 46 SKA LFAA Clock Distribution Network.

14 Firmware

The ADU board is provided with firmware that has been mostly developed by participating research Institutes, listed in Section 4. The ADU structure and the available interfaces and peripherals are described in section 8.2.2

The TPM board is provided with low-level management firmware to perform board configuration and monitoring through the Ethernet interface exploiting a UDP based protocol.

Briefly, the ADU is organised in two main sections: the management and control plane and the acquisition and processing plane. The management plane is built around a FLASH based Lattice MachXO2 CPLD, and includes a 1Gbe Ethernet connection, EEPROM and SPI FLASH memories, and the interface to the Analogue Front End (pre-ADU). The processing plane includes the 16 ADUs, the two FPGAs, the DDR memory and the 40 GbE interfaces.

CPLD firmware is stored on the internal CPLD FLASH memory. It is auto-configuring at board powerup and manages the access to the device registers through the 1GbE control interface, using the UDP based Uniboard Control Protocol. It also provides a master UDP streaming capability, sending over the 1GbE the packets received on the Chip-to-chip (C2C) streaming bus.

FPGA firmware is identical on the two devices. It is composed of two layers: an input-output ring, with physical interfaces (mostly based on vendor specific IPs) encapsulated in a device agnostic wrapper, plus specific generic functionalities (e.g. PPS and clock management, UDP Ethernet layer). The actual signal processing is performed inside a DSP layer, which receives packetised and synchronised samples, and generates packetised processed samples.

A detailed description of the firmware implementation can be found in [PD1], [PD13] and [PD14]. A background IP was registered for the CPLD firmware by Sanitas EG (Appendix F).

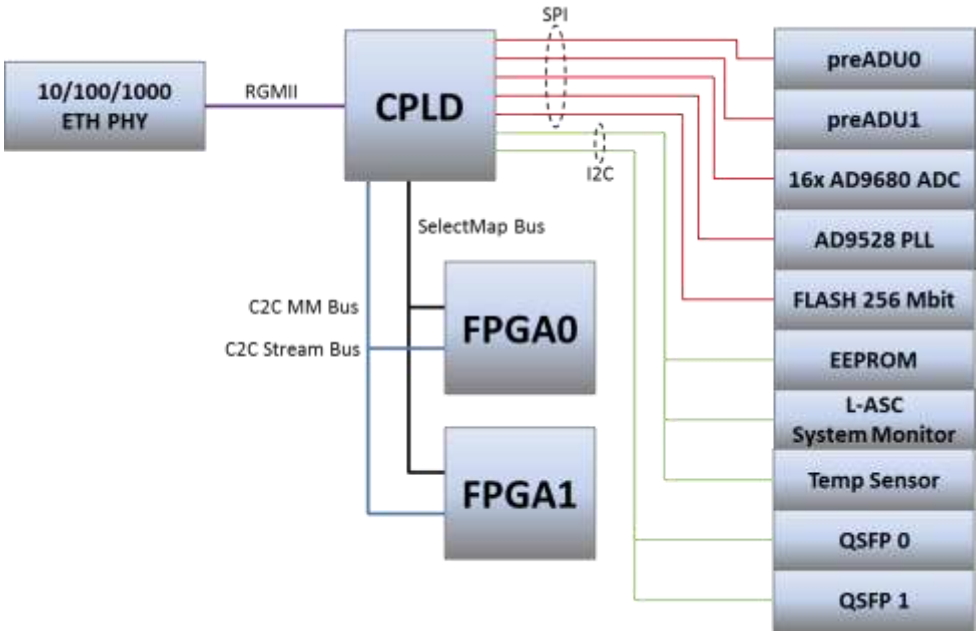


Figure 47 Control plane of the TPM firmware.

14.1 FPGA IP Blocks

FPGA firmware structure is described in detail in [PD13] and shown in Figure 48. It is composed of a ring of physical interfaces and general functionalities, surrounding a DSP layer (Figure 49) performing the actual signal processing. Each block uses standard interfaces for streaming packetised input and output samples, and for control (not shown in the diagram). Stream clock domain is colour coded in the diagrams. Main clock domains are the ADC clock (not oversampled) and the DSP clock (oversampled). Other clock domains are related to the specific hardware interfaces.

Figure 48 refers to the IO ring for TPM 1.2. In TPM 1.5 the DDR interface uses DDR4 standard, and the Ethernet interface uses a 40 GbE core, instead of 4x10GbE cores. Jesd204, DDR and 40GbE use standard Xilinx IP cores. The UDP layer for the 40GbE has been developed internally.

The board control bus (C2C in Figure 47) is translated into an Axi4lite bus to control the internal modules, both in the IO and in the DSP layers.

Time is kept internally with an accuracy of one sample, and locked to the 10 MHz external clock reference. The internal clock is synchronised to the station clock using a PPS signal, on command.

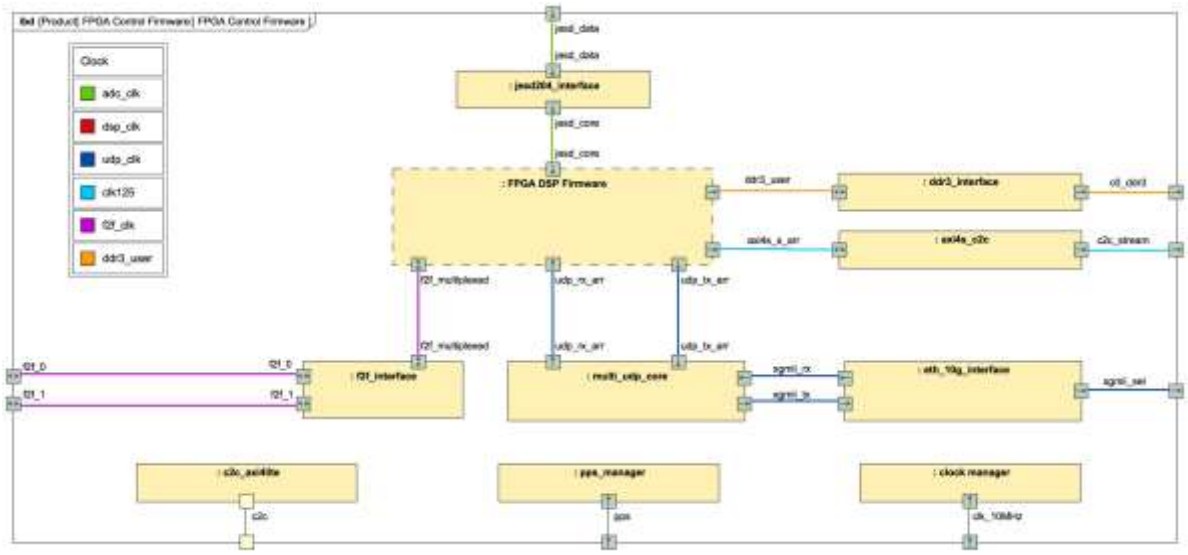


Figure 48 Input/output ring of the FPGA Firmware.

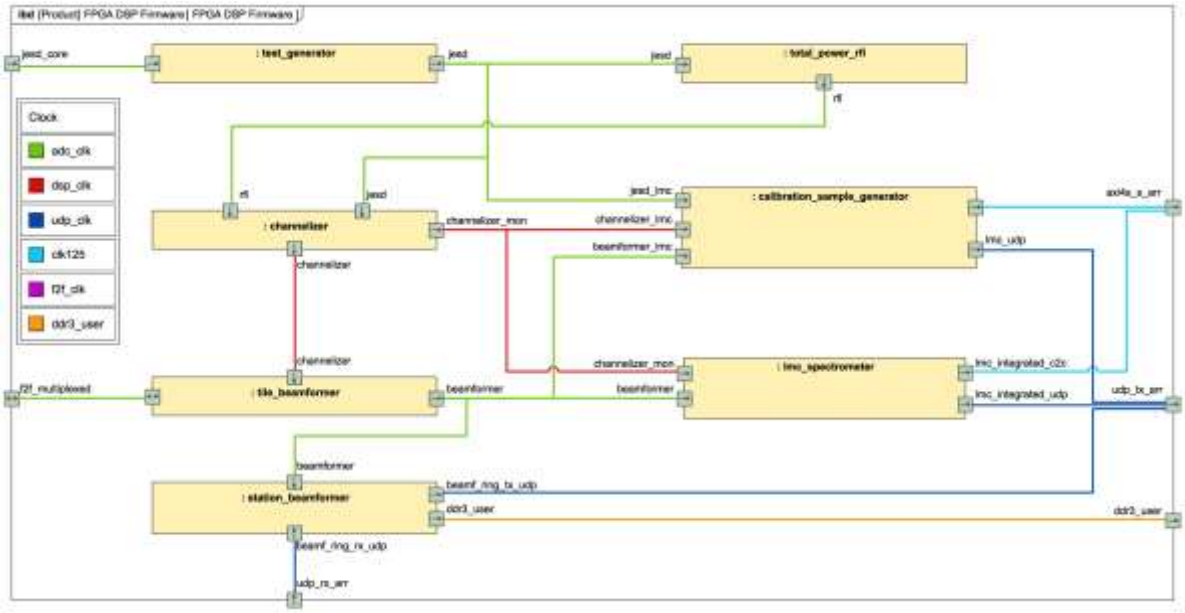


Figure 49 DSP layer of the FPGA Firmware.

The digital signal processing structure is based on a frequency domain beamforming architecture. The digital signal processing structure is based on a frequency domain beamforming architecture. Signal from each antenna is statically aligned to ±1 sample, to correct for cable mismatches, before channelisation. Signals from the individual antennas are channelised with a channel spacing of 781.25 kHz and decimated sample frequency of 925.93 kHz. Fine delay is corrected in the frequency domain by applying a dynamic phase correction to each frequency channel. Receiver and atmospheric gain variations can be corrected by applying a complex calibration factor for each frequency channel. Delay can be specified either as the phase of this factor, or directly as a delay, with the firmware computing the appropriate phase factor for each frequency channel. A delay rate can also be specified, for sidereal tracking.

The beamforming is computed independently for groups of 8 channels. It is possible to select multiple spectral regions in the input band, to generate independent beams, and to use different groups of antennas to implement subarrays. All delays are specified with respect to a station reference point, the same for all tiles. The two FPGAs then exchange data in order to form a partial sum of 16 antennas, for half the processed bandwidth (150 MHz in each FPGA). These partial sums are stored in DDR memory, and organized in frames of consecutive samples by one frequency channel. These frames are then propagated along two daisy chain structures of 16 TPMs (one per FPGA), using the two 40 GbE connections, with each FPGA adding its locally generated partial sum to the frame. At the end of the chain ancillary information is stored in the frame header and the frame is sent to the correlator.

The firmware performs other ancillary functions, shown in the right column in Figure 49.

A test signal generator can be used for debug purposes. It produces two sinusoidal tones, and a Gaussian pseudorandom white noise, with programmable amplitude. This signal can replace the signals from the ADC.

Streams of samples can be extracted from the processing chain and sent, either on the 40G link or on the control 1G link, as UDP packets. Either ADC raw samples, channelized samples for one frequency



channel or beamformed samples can be acquired. This function is used to acquire the channelized samples from individual antennas in order to calibrate the array, or to generate all sky images.

Total power measurement is performed on input samples (on each signal), on the channelized samples (low resolution spectrogram, for one signal), or on the beamformed samples. A RFI detector looks for sudden increases of signal power, both in the wideband raw samples and in the beamformed signal, and optionally flags the affected samples.

A 2-bit version of the beamformed samples can be streamed to an external buffer. This is used to record high temporal resolution data for transient events.

A cyclic buffer in DDR memory stores antenna raw samples for a limited set of antennas, with a depth of a few tenth of a second. This buffer can be frozen, and read back, on an external trigger signal.

15 Software

The Cabinet management is structured over three levels: cabinet level, sub-rack level and TPM level.

The management functions related to a specific level shall be allocated to a corresponding element to allow proper functional separation and maintainability.

Cabinet level functions include power distribution, cooling and other electromechanical interfaces.

Sub-rack level functions include: sub-rack level power distribution (to TPMs), TPM configuration, TPM start-up sequence, synchronization distribution, cooling and status monitoring.

TPM level ones execute the power management and configuration commands and support the TPM system monitoring for internal voltages and temperatures.

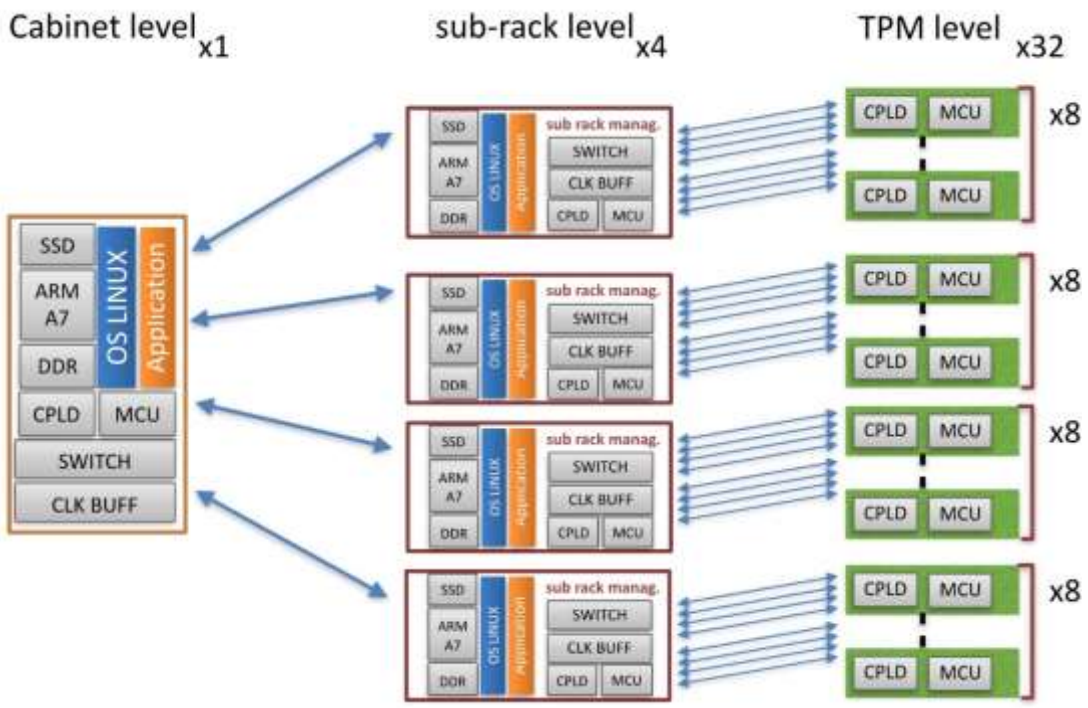


Figure 50: Cabinet management processing architecture.

Each level communicates with a dedicated Ethernet gigabit connection with UDP based protocol for direct memory access and TCP protocol (or similar) for high level operations.

At cabinet and sub-rack levels a complex CPU, with Linux OS shall be present to manage secure TCP based communication with the Telescope Manager and the MCCS applications. The CPUs shall be directly connected on the gigabit network and each board shall also provide a CPLD with a hardwired gigabit UDP interface to allow the low level hardware direct interface and safety critical functions in order to avoid the need of a real time OS on the CPU. Cabinet network is described in more detail in Appendix C.



On the TPM a simple MCU integrate the CPLD functions to execute sequential operations and complex commands received from the management software.

Software at each level manages essentially power up and power down functionalities, initial setup, and safety monitoring. The system as a whole is controlled by an external control infrastructure (Telescope Manager, or TM). The TM commands the cabinet to switch on and off the individual subracks, and each subrack to switch on and off the individual boards. Software at each level can override these commands for emergency shutdown following a dangerous situation. Once the system is initialised it is placed in a standby state, TM directly controls the system elements (e.g. the DSP firmware in the TPMs). Local software functions after initialization are limited

The management board must control at least:

- individual voltages and currents for any power supply
- Voltage at each element inlet, to detect a high contact resistance condition in the power connector
- Temperature in critical points
- Fan speed
- Airflow presence (airflow operated switch).

Software provides safety functions if these parameters assume values outside predefined bounds, and aggregate them for logging by TM.

For the Management board description see Appendix A.

Appendix A Cabinet Management Board (CMB)

The Management board is instantiated in two possible configurations, Rack and Subrack with combined functions.

In the Rack configuration the Management board is boxed in a 1U drawer to provide the following main functions:

- Interfaces with the SKA 40G Ethernet network
- Provides the Rack level 1G local Ethernet Network
- Interfaces with the SKA 10 MHz & PPS Rack synchronization signals and distribute them in the Rack

Provides a Linux-based CPU to execute high level Rack function

Interfaces all rack elements for remote control operation and monitoring

The Rack configuration connectors are grouped on the front side, the Subrack ones are on the two lateral sides. An overview of the board mechanical layout top view is available in Figure 51.

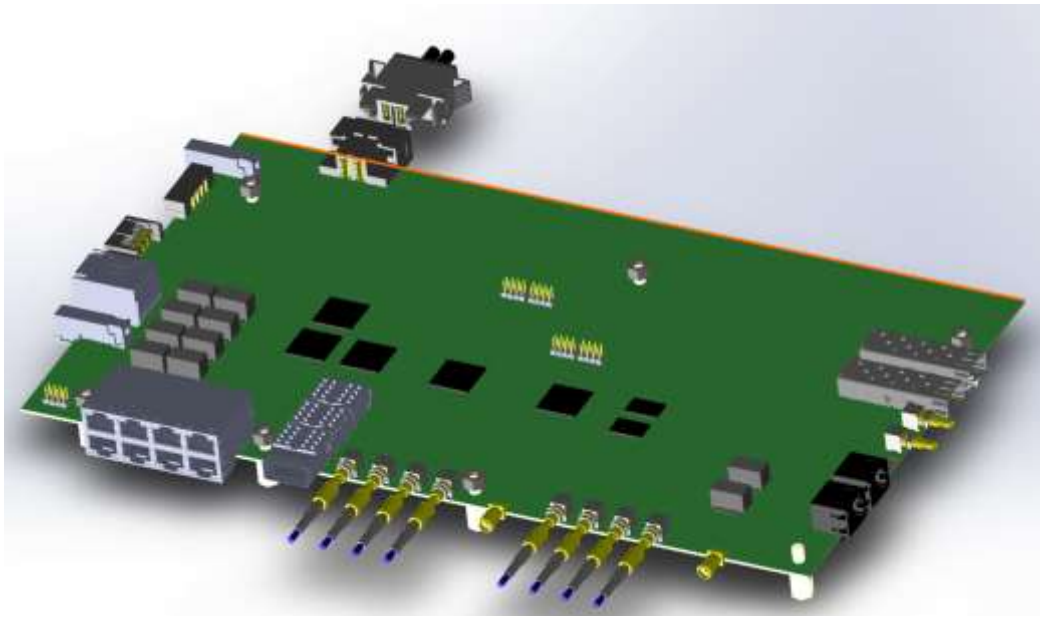


Figure 51 Management board, TOP mechanical layout.

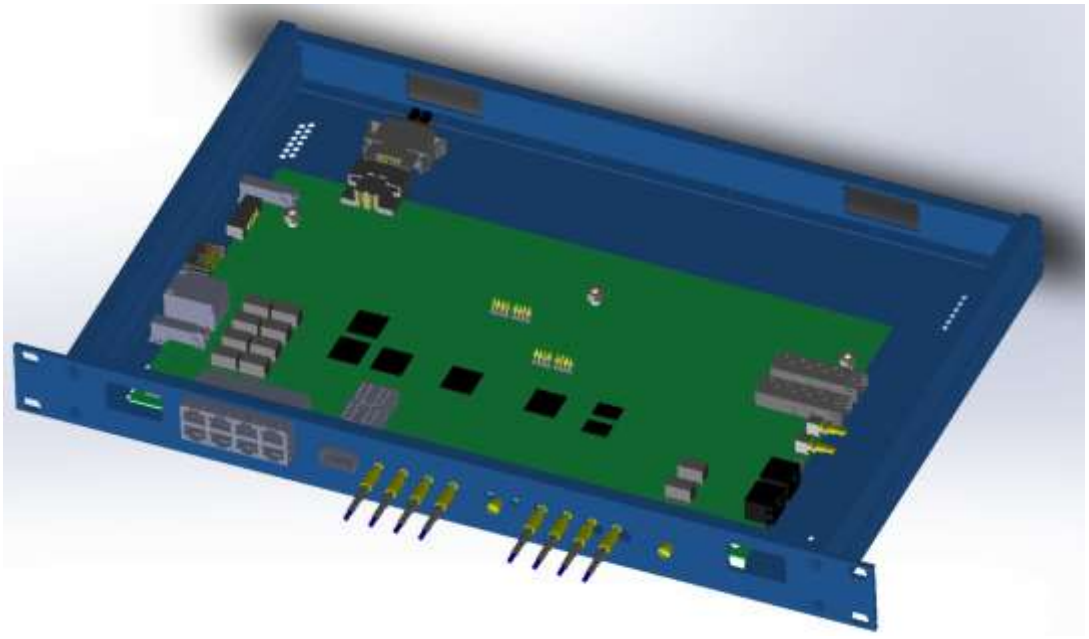


Figure 52 Management board, rack configuration.



Appendix B Cabinet Stack-up

Cabinet elements are summarised in the following Table IV.

Table IV Cabinet Elements.

Description	N.	Rack Unit	Positioning
Processing			
TPM Subrack	4	6	19“ Column
40G Eth switch	2	1	19“ Column
Rack Management	1	1	19“ Column
Powering			
General power, manual	1	1	Side/19" column
Power distributions, actives	-	-	Side/19" column
Mechanics			
External chassis	-	-	-
Internal supports	-	-	-
Cabling elements	-	-	-

Current proposed design is compatible with a standard chassis available on the market. A schematic layout is shown in Figure 53.

The Power distributor element implements the general on/off switch, with manual activation and the required safety passive protections. The power distribution unit manages all the controlled switches that can power all the other cabinet elements, with exception of the management board that shall be always powered.

The TPM sub-rack will be possibly coupled with the 40G Ethernet switch placed in the middle to implement a complete station module. With this approach the 40G QSFP connection are short and local and all the TPM of a single station are connected to the same switch to assure communication efficiency.

In Figure 53, the beige cabling units are empty space for fibres and general cabling to allow maintenance capability and the possibility to extract a single TPM without other cable removal. The cabinet management and the 1Gbit management switch (optionally considered but not in the baseline design) can be placed in the middle or everywhere in the 19” column. The middle position can be optimal for clock cabling and network connections to each sub-rack.

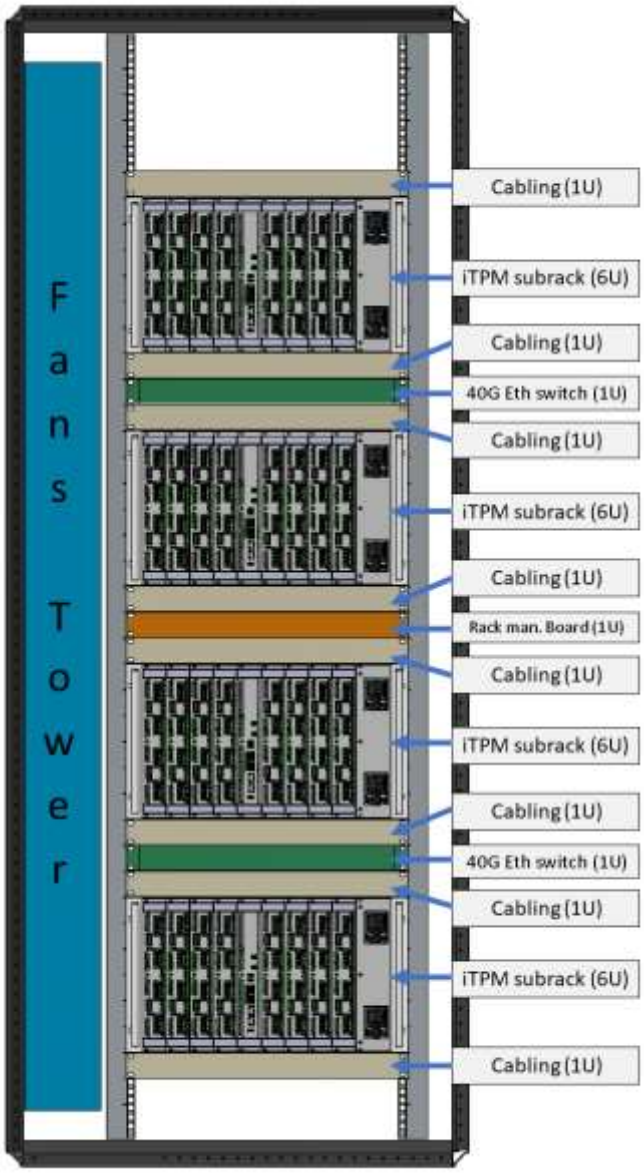


Figure 53 SKA LFAA Cabinet stack-up.



Appendix C LFAAA SPS Network

A general network architecture for LFAA SPS is presented in [PD1]. An initial proposal for how to organize the network structure in the LFAA SPS, both for the control network and for the data transport network, assign MAC and IP addresses and manage the LFAA network is discussed in [PD15].

SPS is organized into 256 SPS cabinets, each one implementing the beamforming electronics for two stations. 148 cabinets are hosted in the Central Processing Facility, and the remaining 108 into 36 Remote Processing Facilities. Cabinets are grouped into groups of 4 (CPF) or 3 (RPFs) providing some backup routing and the possibility of reducing network complexity [PD1].
The network serves two purposes:

- Local Monitor and Control: MCCS monitors the status of all equipment, and provides calibration, pointing, and sequencing commands to control the system and to execute the astronomic observations. Expected data rate is modest, even when 8192 individual TPMs must be controlled.
- Data flow: partial beams are produced by each TPM, summed together into a station beam, and transmitted to CSP. Calibration spigots and transient buffer samples are also sent from TPMs to the MCCS. Data rate is high inside each cabinet (23 Gb/s per TPM), between the cabinet and CSP (23 Gb/s per cabinet) and between the cabinet and MCCS (22-27 Gb/s per cabinet).

Data flow uses a 40G/100G network. Two high speed switches are present in each cabinet. One of the switches is connected to MCCS and to SPS, using two separate links.
LMC flow uses a standard 1Gb network inside each cabinet. This network is connected to MCCS both with a 1Gb link (active in any condition) and through the Data network when the high speed switches are active.
Front Node equipment (FNCH) is seen as a single node per station (TBC), which is physically connected through a 1Gb optical SFP connection. The node is part of the cabinet net but is controlled directly by MCCS. SPS acts only as a routing path.
The physical structure of the cabinet network is shown in Figure 54. The switch-to-switch interconnection uses QSFP+ copper cables. All other 100GbE connections use optical QSFP+ cables. All 40GbE connections use passive copper cables. The 1GbE connection to FNDH uses SFP optical LR transceivers. All other 1GbE use copper cables. The 10GbE connection between the cabinet switch and the CMB uses two lanes of a QSFP passive copper cable.

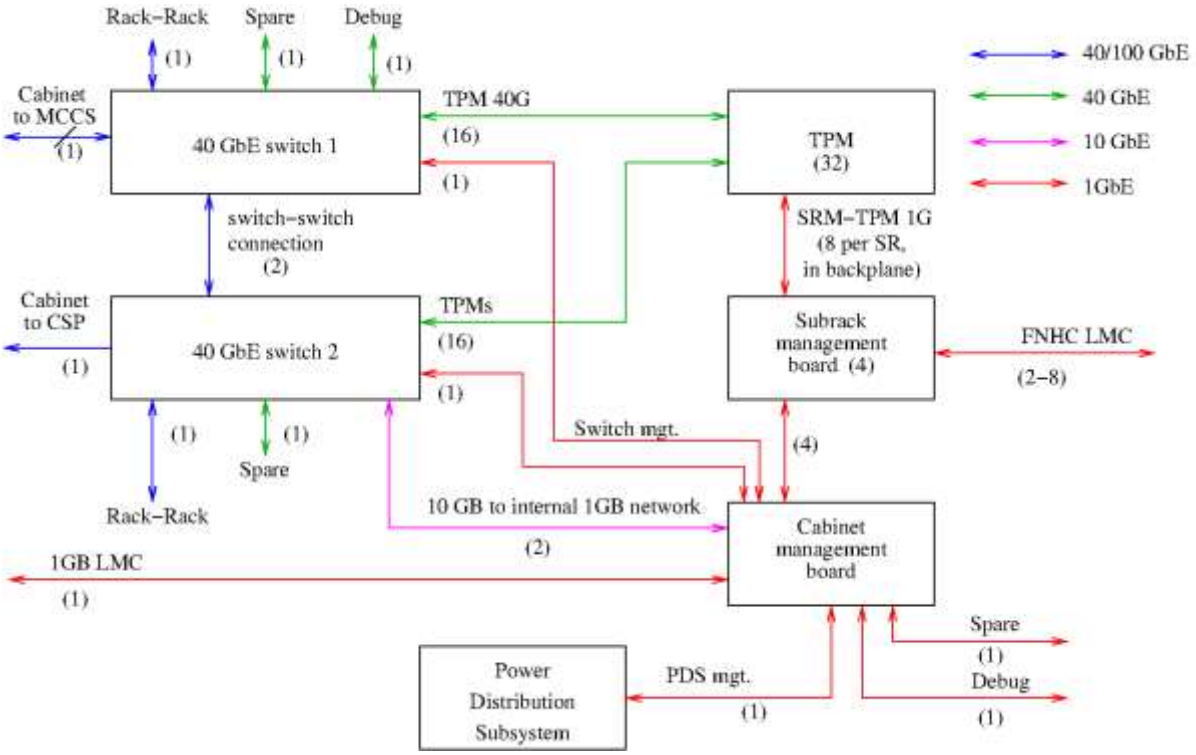


Figure 54 Cabinet physical network.

Rationale of the proposed network structure

MCCS must be able to correctly address resources for each antenna and station. These resources are identified by their IP address, on the software side, and by their physical location in the CPF or RPF, on the hardware side. The physical to software mapping must be stable and predictable.

All devices have a serial number, which must be visible, in human and machine readable format, in a label sited in an easily visible location (SKA-SYS_REQ-2573). Devices which can be addressed on the net have one or multiple ports, each one with a unique MAC address. At least one port per device has a factory set MAC address, which is also reported on a label. Some ports (e.g. high speed interfaces on FPGAs) have configurable MAC address, which is arbitrarily assigned in firmware, by the control software.

If a device has multiple ports, usually one will be considered the “main” one. This is the one which allows an external controller to check (or set) the remaining ports.

The MAC address and IP address of each interface must be defined in a unique way, after power up. A list of serial numbers and MAC addresses will be maintained in a central database, as part of the Logistics Analysis and Configuration structure. This is however a very error prone procedure, if it is the only way to map physical locations to hardware. So an independent way to assign IP addresses is highly desirable.

The IP/MAC assignment procedure must:

- minimize operator work
- minimize possibility of errors

- guarantee that no deadlock situations occur
- allow exchanging of identical boards without significant operator work
- allow unique addressing based on geographic position within cabinet
- minimize (or avoid) identifications based on the MAC address. MAC address in the Configuration structure will be cross checked, and inconsistencies reported (and resolved).

The operator must follow a simple and easy procedure when installing or moving the boards, with a way to check that everything is correct.

In [PD2] it is suggested that the SPS network is split into separate class D subnets, with each subnet including a group of 4 (or 3) cabinets. As there are more than 100 IP nodes per cabinet, it is more appropriate to have a single network per cabinet. Separating the LMC and Data networks in each cabinet is also advisable, to prevent data flooding from a defective FPGA to stop the LMC functionalities. This implies that cross network (level 3) routing is implemented in the CMB and in the cabinet switches.

The proposed network structure is shown in Figure 55. Both requirements and mechanisms for assigning IP/MAC addresses at cabinet and subrack levels are illustrated in [PD15].

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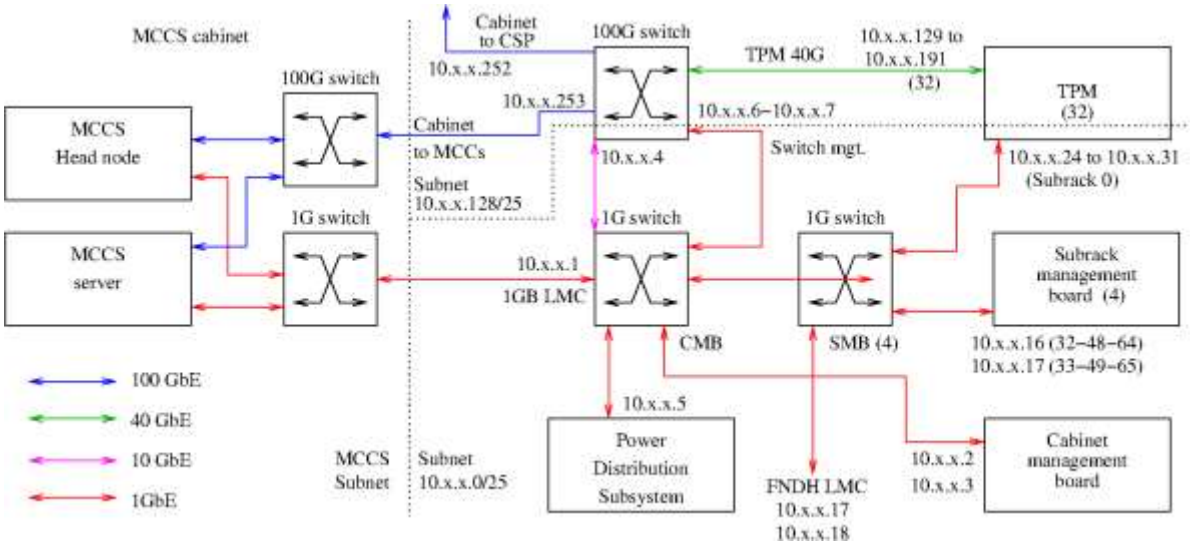


Figure 55 Logical partition of the cabinet network.

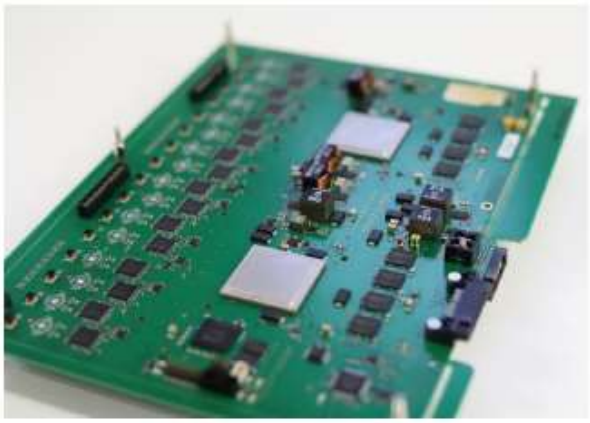
Appendix D ADU 1.6 Board

- ✓ 32 RF input, 50Ohm
- ✓ Analog Devices AD9695, 14-bit high performance ADCs
- ✓ Digital beamforming
- ✓ 50MHz – 650MHz optimized for SKA analog band, ADC and board capabilities up to 2GHz
- ✓ Maximum Sampling Rate 1.25GHz
- ✓ Channel isolation > 60dB
- ✓ ENOB > 7.89 with 8-bit channels configuration
- ✓ JESD204B Subclass 1, 2x16 lines
- ✓ Management MCU, ARM Cortex-M0™
- ✓ 2 Xilinx UltraScale+ XCKU9P FPGAs
- ✓ Compact size, 6U format compatible
- ✓ 2x 40G Ethernet interfaces (QSFP)
- ✓ 2x 64-bit DDR4-1600
- ✓ Management instant ON Lattice CPLD with Ethernet Gigabit Link
- ✓ System Monitor
- ✓ 256Mbit SPI on board FLASH for multiple FPGA configuration
- ✓ High efficient Power Distribution System, single input DC supply
- ✓ EMI verified
- ✓ 65Watt load with test application

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iTPM ADFE 1.6
Multi-Channel Digital Beamformer



Description

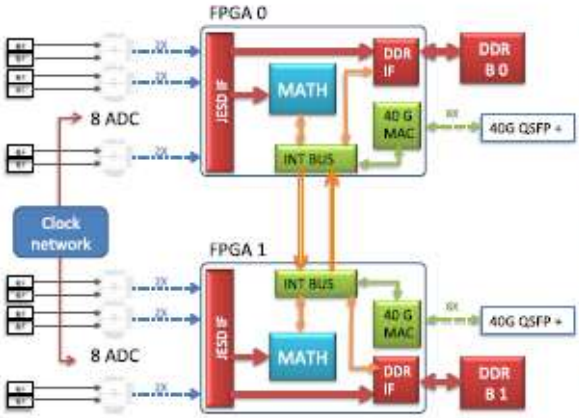
The iTPM ADFE (italian Tile Processor Module Analog to Digital Front-End) 1.6 is responsible for Analog to Digital conversion and pre-processing of a **multi-channel** source managing up to 32 analog inputs with sampling frequencies from 700MHz up to 1GHz (32 8/12-bit channels are supported).

Best in class 14-bit AD converters, recent 16nm FPGA, 40Gbit Ethernet optical links have been selected focusing on the best commercial compromise between quality, performance and power consumption. Compact board size, low noise clock network, advanced 14-layer board build-up, Ethernet based management features (including health monitoring capability), high efficiency and low noise power distribution system complete the main board features.

An accurate board design allows an high-density RF interface with **superior performance** with high linearity, low interference between channels to meet really challenging requirements.

The board has been developed in collaboration with INAF (National Institute for Astrophysics) and Oxford University in the frame of the Square Kilometer Array (SKA) (https://skatelescope.org) **international project**, and is used within the antenna receiver module of the radio telescope. The **beamforming** technique is successfully adopted in the directional signal reception, thanks to this powerful board.

Board Specifications and Characteristics



Thanks to the JESD204B interface all the ADs are source synchronous and can be phase aligned with a 10MHz external reference and PPS.

Two identical FPGAs interface eight dual channel ADs with JESD204B, 16 lines available for each FPGA, 2 lines for each AD, 64-bit DDR4 memory and a 40G Ethernet interface with a QSFP+ connector.

A management CPLD is present with a dedicated Ethernet Gigabit link for loading firmware and monitoring temperature and voltage over 40 internal points.

Component Description	Component
Management CPLD	Lattice Semiconductor LCMXO3L-9400E
Management FLASH	2x 256Mbit SPI
Management MCU	ATSAMD21J18A
FPGA	2x Xilinx XCKU9P-1FFVE900E
FPGA Memory	2x 2GByte DDR4-1600(*)
Analog to Digital Converter	16x Analog Devices AD9695BCPZ-1300
Front Panel Connectors	2x QSFP
	SMA, external 10MHz reference
	SMA, PPS
	Input Supply
	RJ45 Gigabit
RF INPUT Connectors & GPIO	4x ISORATE IP5 08
	2x ERF8 010
Internal GPIO	2x 2 GPIO
Debug Connector	FPGA JTAG
Power Supply	12-24 VDC
Power Consumption	Up to 150W
Working Temperature	+5°C / +55°C
Board Size	233mm x 170mm x 31mm

V1.1

(*) Upgradable to 2x 8GByte DDR4-2400

In this specific configuration the heat dissipator is not included.

Sanitas EG reserves the right to change specifications without notice

Appendix E Subrack Electronics

- ✓ Kit composed by Backplane board, Management board, Power-on Adapter, FANs
- ✓ Structure to integrate 8 iTPM–ADU boards in the Cabinet (chassis not included)
- ✓ Two Redundant Power Supplies 110V-220V AC
- ✓ Air based cooling support
- ✓ Absorbed current value monitoring
- ✓ Power ON/OFF capability of each iTPM-ADU board
- ✓ CPU with Linux OS
- ✓ 2 Ethernet gigabit IFs
- ✓ Easy accessible connectors

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SKA
LFAA Subrack Kit
(without chassis)

Description



The LFAA Subrack system is the basic structure required to integrate the iTPM–ADU boards within the Rack: the iTPM-ADU is the main board managing Analog to Digital conversion and pre-processing of a multi-channel source in the LFAA (Low Frequency Aperture Array) of the SKA (Square kilometre Array) telescope (https://skatelescope.org) .

The Subrack is composed by:

- **Backplane board** to move all the required services, needed by iTPM-ADU, from the front-panel to the opposite side
- **Management board**, plugged on the Backplane, providing relevant functions as interfacing the Rack Ethernet network to the iTPM-ADUs, distributing/regenerating the synchronization signal to the iTPM-ADUs, managing/monitoring the Subrack power supply, power distribution, FANs, providing a Linux-based CPU
- **Commercial power supplies**
- **Adapters board** to interface the power supplies
- **4 commercial fans**

Kit Functionalities

Each Subrack provides the following functions:

- iTPM-ADU interface on the backplane for the Power, management Gigabit Ethernet, reference clock and PPS and single wire configuration access
- Mechanical compatibility with 8 LFAA iTPM-ADU 1.6 boards
- Integrated air based cooling
- Power ON/OFF capability of each iTPM-ADU board with monitoring and safety embedded functions
- CPU with Linux OS to manage high level operations
- Subrack level Gigabit ethernet switch functions, including 2 copper and 2 optical front panel interfaces, 8 copper interfaces on the backplane for the iTPM and internal direct connection to the OS CPU and the CPLD with 10G internal bus.
- Two Redundant Power Supplies 110V-220V AC
- Complete firmware based subrack-level monitoring and safety capability
- Reference Clock distribution with Jitter cleaning and PPS phase measurement
- Debug and Trace interface for advanced SW debug capabilities

Deliverables

The physical kit includes:

- 1 Backplane board
- 1 Subrack Management board
- 2 Commercial power supplies
- 1 Power supplies adapters board
- 4 Fans
- Low level firmware (management BIOS) and support for Debian Linux OS versions
- 1-year warranty

- Chassis not included in this kit version

Sanitas EG reserves the right to change specifications without notice

Appendix F Intellectual Property Declaration

The following pages provide the Intellectual Property declaration from Sanitas EG.

SKA Intellectual Property Rights (IPR) Notification Form

Please indicate your response to the listed requirements

Please use one form for each IPR you wish to notify

No	Requirement	Response
1	Description of technology or work in relation to which IPR is said to exist. *(Use continuation sheets if necessary.)* *(This should include a brief description of what the function of the technology is and of how such technology carries out that function.)*	Ethernet management and test interface, including Xilinx SMAP test interface. This IP allow the management, test and quality assurance of FPGA based complex design
2	Brief outline of the relevance of this technology or work for the SKA Project. *(Use continuation sheets if necessary.)* *(This should include the identification of the products in which the technology or work is used – reference to an item in the approved Product Breakdown Structure is required here)*	This IP allow to efficienlty manage the large number of TPM remote FPGA base system and to estimate the contribute to the MTBF of the FPGA design

Document No.: SKA-GOV.CON.IPR-SKO-FRM-001
Revision: 2
Date: 2017-10-20

Restricted once completed
Author: Colin Greenwood
Page 1 of 5

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Viale del Parco Mellini 84
00136 Roma – ITALY
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Date: 2020-05-21

3	Details of any filings for patents, utility models, registered designs etc. made in respect of the technology or work. *(This should include the application number of the right, any publication number and the number of any granted right.)*	Patented, not renewed, in 2010
4	Date on which first filings for patents, utility models, registered designs etc. in respect of the technology or work were made.	About 2006, request for patent date
5	Location of patent/design or trade mark office in which first filing(s) for the IPR was/were made. *(This will be a national or international trade mark, patent or registered design office such as the EPO, OHIM, USPTO or a national office (e.g. the German national patent office).)*	Italy
6	Countries/Jurisdictions for which patent, utility model, registered design etc. protection is or has been sought.	Italy



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7	Type of IPR. *(State whether patent, copyright, design right, registered design, utility model, design patent, semiconductor topography right, database right, confidentiality rights or rights in trademarks or other rights.)*	☐ Patent ☐ Copyright ☒ Design Rights ☐ Registered Design ☐ Utility Model ('Innovation patent') ☐ Design Patent ☐ Semiconductor topography rights ☐ Database rights ☐ Confidentiality rights (Trade Secrets) ☐ Trademarks ☐ Other rights
8	Date of creation of the technology or work in which the IPR is said to exist.	2006 and 2010 for ethernet extension
9	Date on which IPR is said to have come into effect and become enforceable. *(This will either be the date of grant for a registered IPR or the date of creation of a physical embodiment of the work in relation an unregistered IPR.)*	Design start
10	Date on which IPR is said to cease to have effect and become no longer enforceable.	Design and production ended
11	Is the IPR said to be Background IPR or Foreground IPR? *(These are as defined in the IP Policy)*	☒ Background IPR ☐ Foreground IPR ☐ N/A (Third Party IPR)
12	If the IPR is said to be Background IPR but was created after you became an SKA Contributor then please provide a brief explanation as to how it came to be created outside the SKA Project.	Created before

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SKA Intellectual Property Rights (IPR) Notification Form

13	Countries/jurisdictions in which IPR is said to have effect.	All
14	Identify any key requirements as to territory, exclusivity, field of use and exclusions from field of use, duration, necessary business relationships, etc., that you would likely seek to impose on any prospective licensee (including the SKAO). *(Please ensure that any terms that are to be imposed on the use of the IP in the SKA appear here explicitly.)*	na
15	Details of individual creators of the technology or work in relation to which IPR is said to exist. *(State the names and addresses of all those persons said to have created the technology or work. List no more than five persons.)*	Sanitas EG employee, Monica Alderighi Sergio d'angelo

SKA Intellectual Property Rights (IPR) Notification Form

16	Name of IPR owner.	Sanitas EG srl
17	Postal Address of IPR owner.	Viale Restelli 3, 20124, Milano (IT)
18	Contact Details for IPR owner. *(State the name, email address and telephone number of the contact person.)*	Sandro Pastore, sandro.pastore@sanitaseg.it, cell +39 320 0945069

19	Details of any licences of the IPR already granted to third parties. *(State the name of licensee, licensed activity, date and term of licence for the IPR being registered here.)*	Name of licensee: na Licensed application: na Date of commencement: na Term of licence: na
20	Deleted	
21	Details of any licences that are likely to be granted to third parties in respect of the IPR in the future. *(State the name of prospective licensee, licensed activity, likely date and term of licence.)*	Name of prospective licensee: na Licensed application: na Likely date of commencement: na Term of licence: na



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22	Status of embodied IPR ('Third Party IPR') Permissions. *(State details of any known IPR not owned by you which use of this technology or work would be likely to infringe absent an appropriate licence. Details to include nature of the embodied IPR and details of the owner of that IPR together with details of any approaches made to the owner to obtain any necessary licence(s).)*	na
23	Author Record. *(State the name and job title of the person who created the record.)*	Sandro Pastore, Sanitas EG, CEO
24	Date of Record. *(State the date that this record was last updated.)*	23 November 2017
25	Signature.	